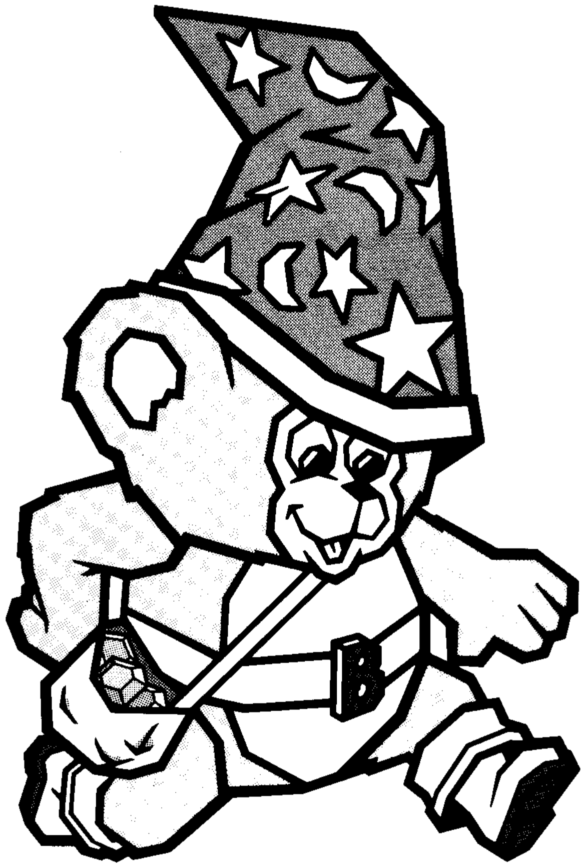


NOTE
Remove this staple to separate the schematic diagrams from the Troubleshooting Guide.

Schematic Package Supplement to

CRYSTAL CASTLES™

Operators Manual

Includes
Troubleshooting Guide

7M

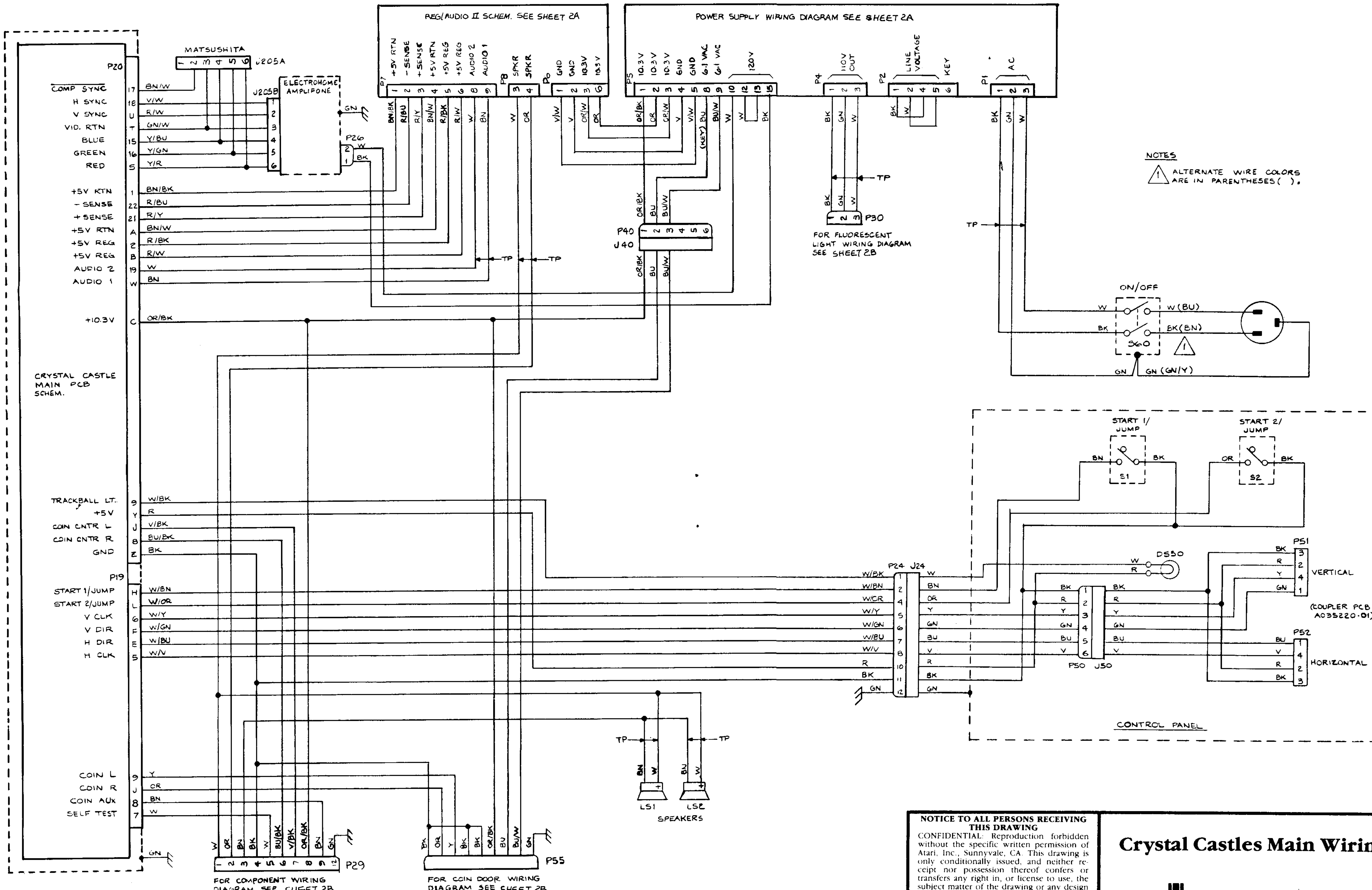
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Table of Contents

NOTE

A Crystal Castles Troubleshooting Guide is included as part of this Schematic Package Supplement. The Troubleshooting Guide contains Atari CAT Box troubleshooting procedures.



Crystal Castles Main Wiring Diagram

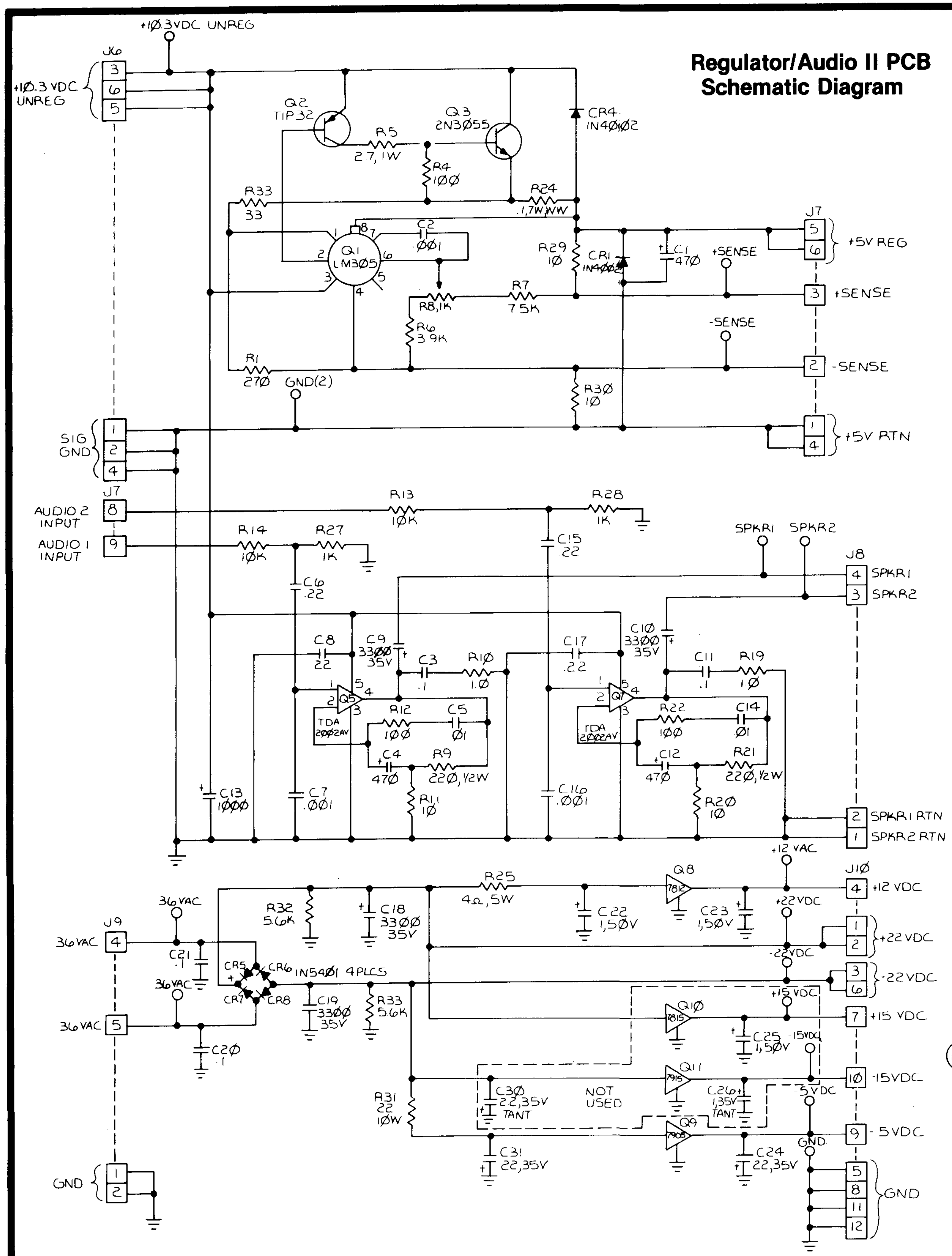
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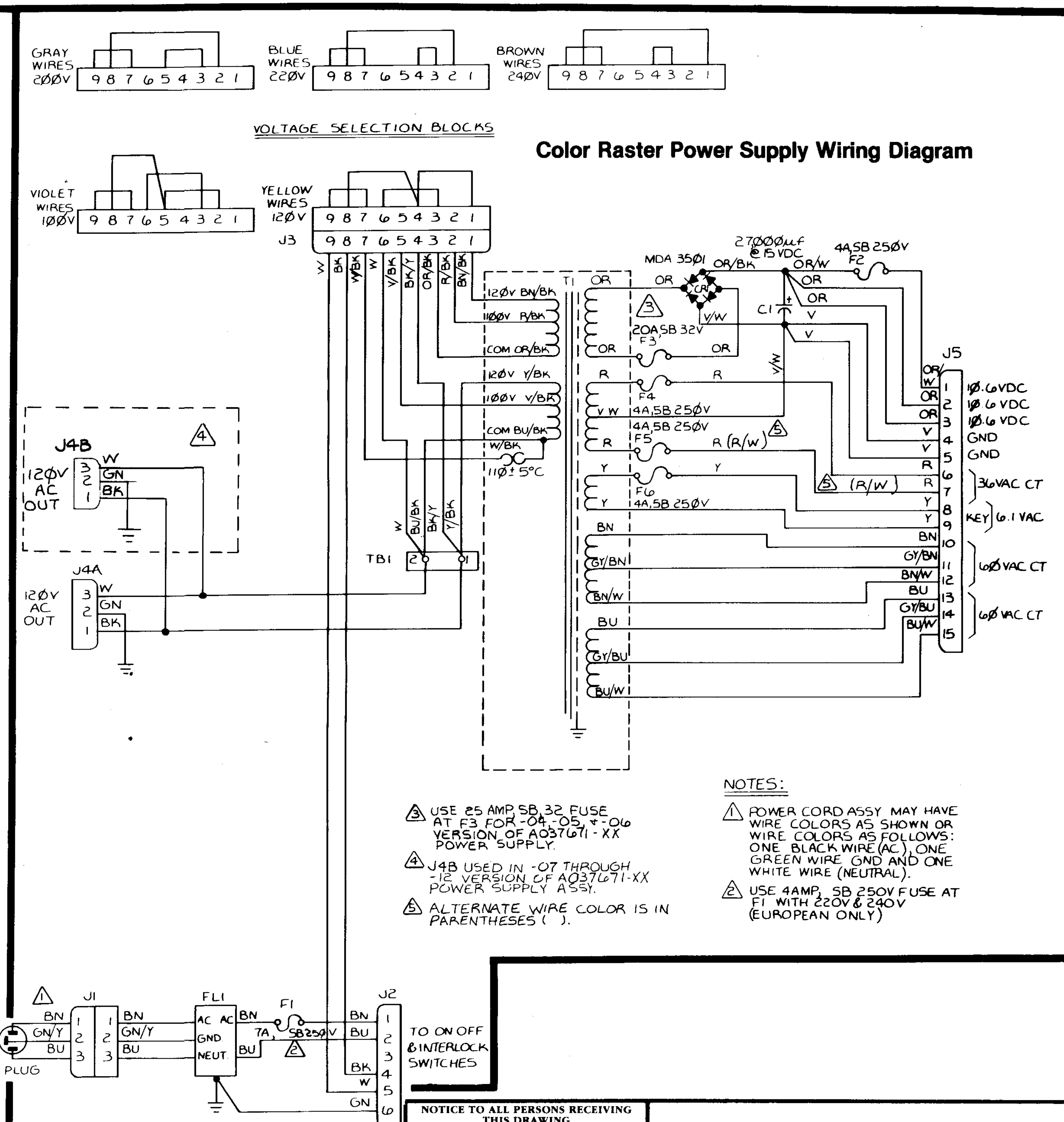
SP-241 Sheet 1B

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Regulator/Audio II PCB Schematic Diagram



Color Raster Power Supply Wiring Diagram



3 USE 25 AMP, SB, 32 FUSE AT F3 FOR -04, -05, & -06 VERSION OF A037671-XX POWER SUPPLY.

4 J4B USED IN -07 THROUGH -12 VERSION OF A037671-XX POWER SUPPLY ASSY.

5 ALTERNATE WIRE COLOR IS IN PARENTHESES ( ).

NOTES:

1 POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE GND AND ONE WHITE WIRE (NEUTRAL).

2 USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)

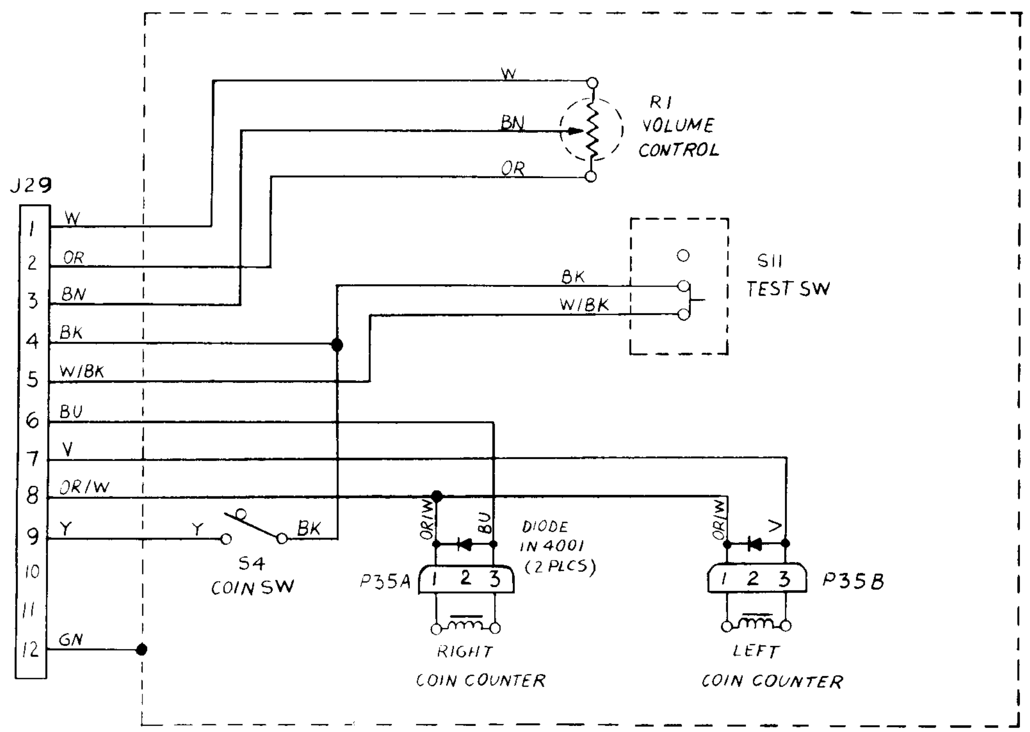
Crystal Castles Regulator/Audio II PCB and Power Supply Diagrams

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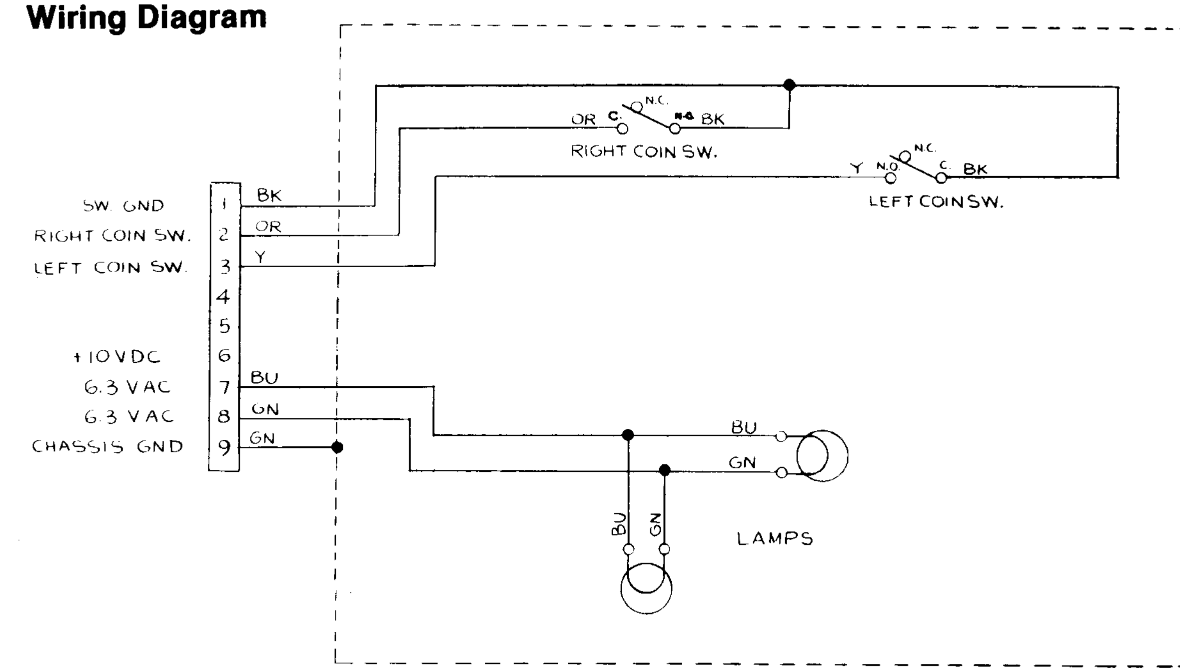
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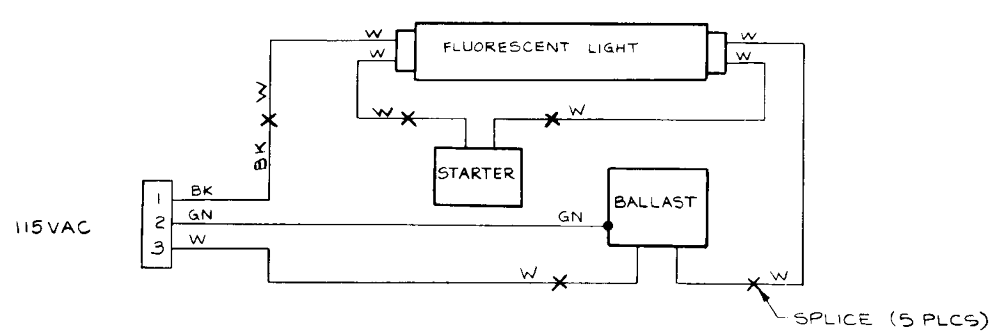
Utility Panel Wiring Diagram



Coin Door Wiring Diagram



Fluorescent Light Wiring Diagram



Crystal Castles Game Interfaces

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Crystal Castles Memory Map

HEXA-DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	READ/WRITE	DATA BUS SIGNAL LINES D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	W	X	X	X	X	X	X	X	X	X COORDINATE
0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	W	D	D	D	D	D	D	D	D	Y COORDINATE
0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	R/W	D	D	D	D					BIT MODE
0003–0BFF	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	WORKING RAM (DRAM)
0C00–7FFF	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	SCREEN RAM
8000–8DFF	1	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	WORKING RAM (STATIC)
8E00–8EFF	1	0	0	0	1	1	1	0	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	MOTION OBJECT BUF 2
8F00–8FFF	1	0	0	0	1	1	1	1	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	MOTION OBJECT BUF1
															0	0	R/W	D	D	D	D	D	D	D	D	MOTION OBJECT PICTURE
															0	1	R/W	D	D	D	D	D	D	D	D	MOTION OBJECT VERTICAL
															1	0	R/W	D								MOTION OBJECT PRIORITY
															1	1	R/W	D	D	D	D	D	D	D	D	MOTION OBJECT HORIZONTAL
9000–90FF	1	0	0	1	0	0	X	X	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	NOVRAM
9400–9403	1	0	0	1	0	1	0	X	X	X	X	X	X	X	A	A	R									TRAK-BALL
4600	1	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	R									IN0
																	R								D	COIN R
																	R							D		COIN L
																	R						D			COIN AUX
																	R					D				SLAM
																	R				D					SELF TEST
																	R			D						SPARE
																	R		D							JMP 1
																	R	D								JMP 2
9800–980F	1	0	0	1	1	0	0	X	X	X	X	X	A	A	A	A	R/W	D	D	D	D	D	D	D	D	CI/O 0
9A00–9A0F	1	0	0	1	1	0	1	X	X	X	X	X	A	A	A	A	R/W	D	D	D	D	D	D	D	D	CI/O 1
9A08																							D	D	D	OPTION SW
																						D				SPARE
																					D					SPARE
																				D						COCKTAIL
9C00	1	0	0	1	1	1	0	0	0	X	X	X	X	X	X	X	W									RECALL
9C80	1	0	0	1	1	1	0	0	1	X	X	X	X	X	X	X	W	D	D	D	D	D	D	D	D	HOR SCROLL CNTR LOAD
9D00	1	0	0	1	1	1	0	1	0	X	X	X	X	X	X	X	W	D	D	D	D	D	D	D	D	VERT SCROLL CNTR LOAD
9D80	1	0	0	1	1	1	0	1	1	X	X	X	X	X	X	X	W									INTERRUPT ACKNOWLEDGE
9E00	1	0	0	1	1	1	1	0	0	X	X	X	X	X	X	X	W									WDOG
	1	0	0	1	1	1	1	0	1	X	X	X	X	A	A	A	W								D	OUT 0
9E80														0	0	0	W								D	TRAK-BALL LIGHT
9E81														0	0	1	W								D	
9E82														0	1	0	W								D	STORE LOW
9E83														0	1	1	W								D	STORE HIGH
9E84														1	0	0	W								D	SPARE
9E85														1	0	1	W								D	COIN CNTR R
9E86														1	1	0	W								D	COIN CNTR L
9E87														1	1	1	W								D	BANK0–BANK 1
	1	0	0	1	1	1	1	1	0	X	X	X	X	A	A	A	W					D				OUT 1
9F00														0	0	0	W					D				$\overline{AX}$
9F01														0	0	1	W					D				$\overline{AY}$
9F02														0	1	0	W					D				$\overline{XINC}$
9F03														0	1	1	W					D				$\overline{YINC}$
9F04														1	0	0	W					D				PLAYER 2
9F05														1	0	1	W					D				$\overline{SIRE}$
9F06														1	1	0	W					D				BOTHRAM
9F07														1	1	1	W					D				BUF1/$\overline{BUF2}$
9F80–9FBF	1	0	0	1	1	1	1	1	1	X	A	A	A	A	A	A	W	D	D	D	D	D	D	D	D	COLORAM
A000–FFFF	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PROGRAM ROM

Crystal Castles Memory Map

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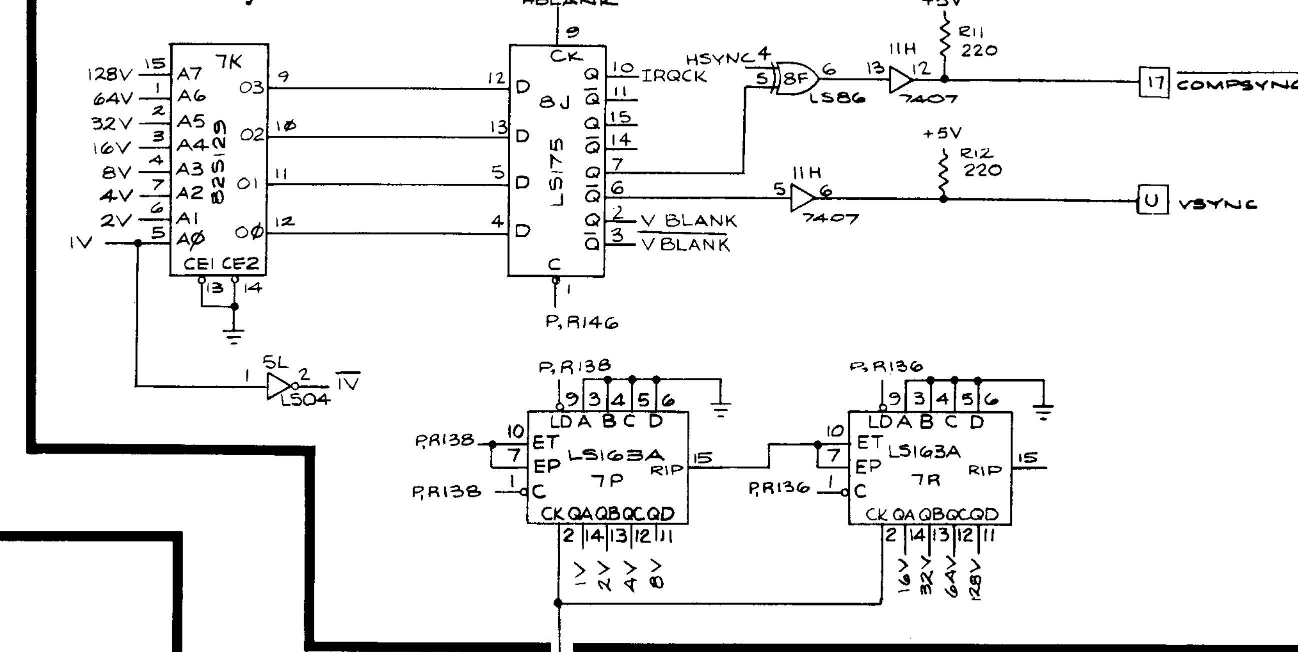
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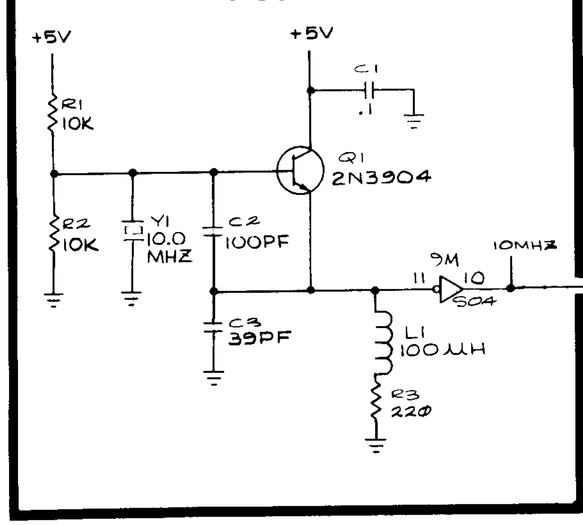
Connector Symbols

1. ☐ DENOTES J20 CONNECTOR.
2. ▢ DENOTES J19 CONNECTOR.
3. ○ DENOTES TEST CONNECTOR.

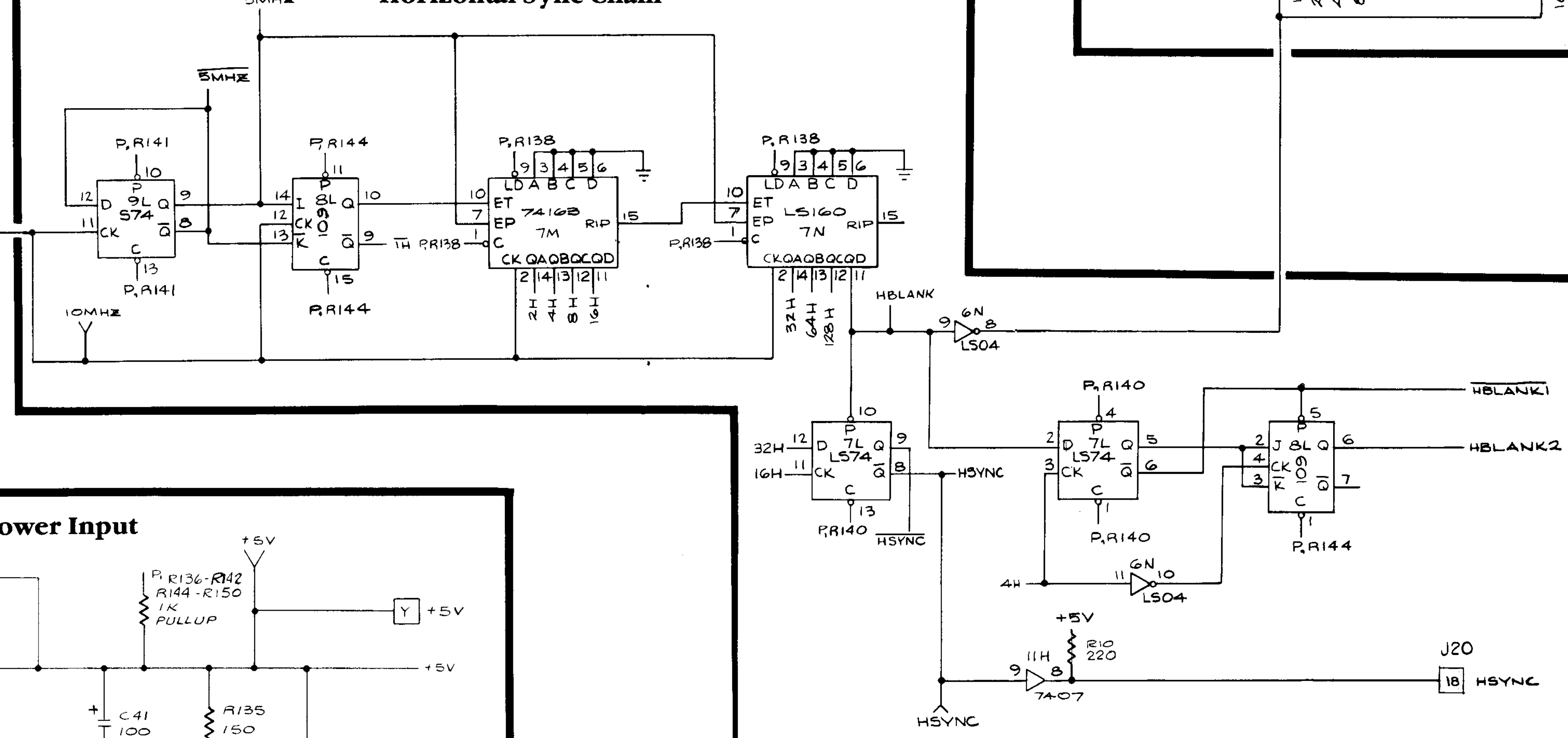
Vertical Sync Chain



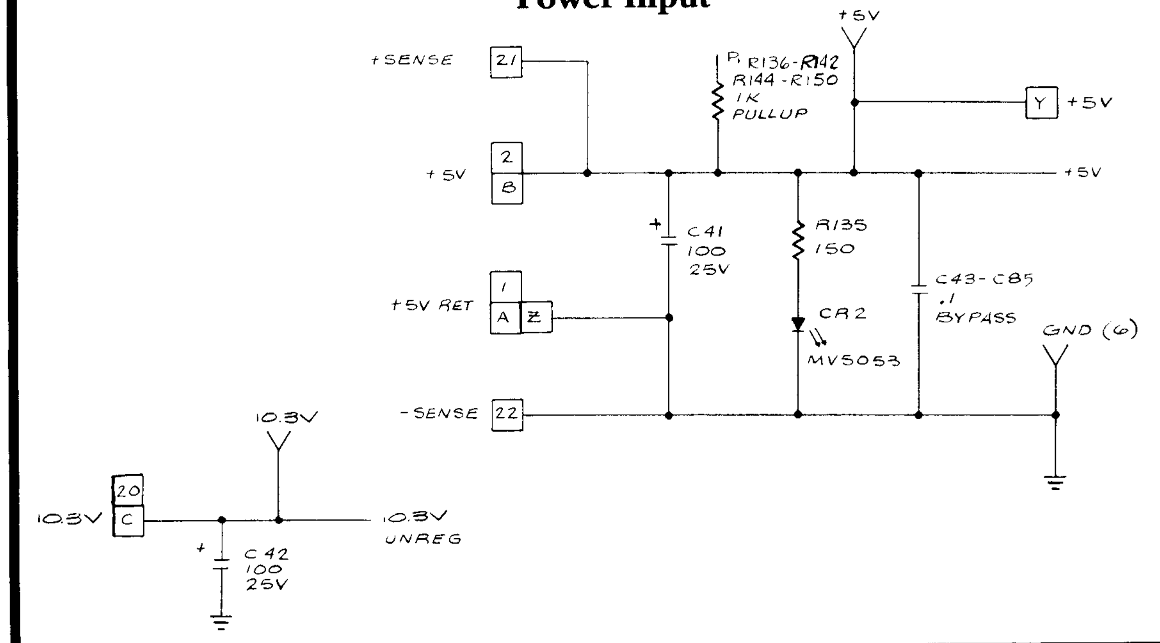
Clock



Horizontal Sync Chain



Power Input



Crystal Castles PCB Schematic Diagram

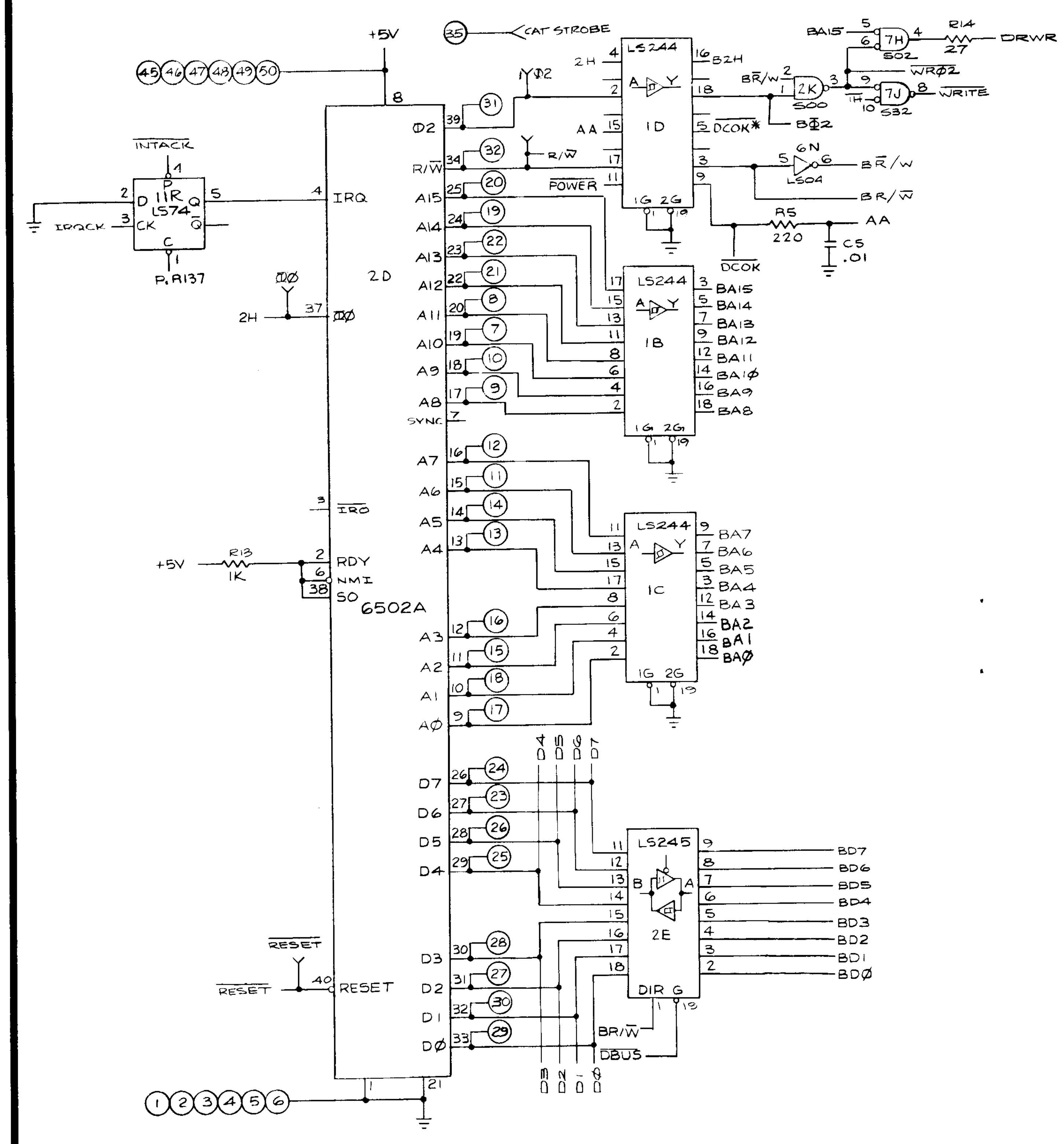
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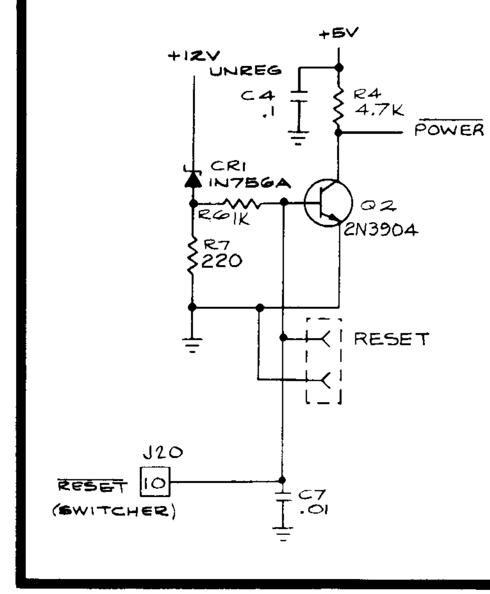
SP-241 Sheet 3B

2nd printing

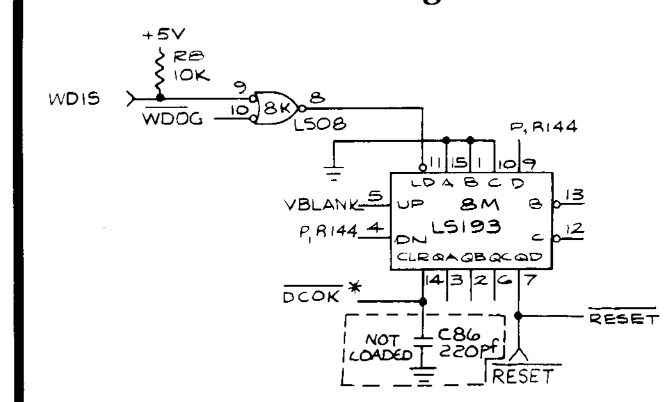
Microprocessor



Power-On Reset



Watchdog



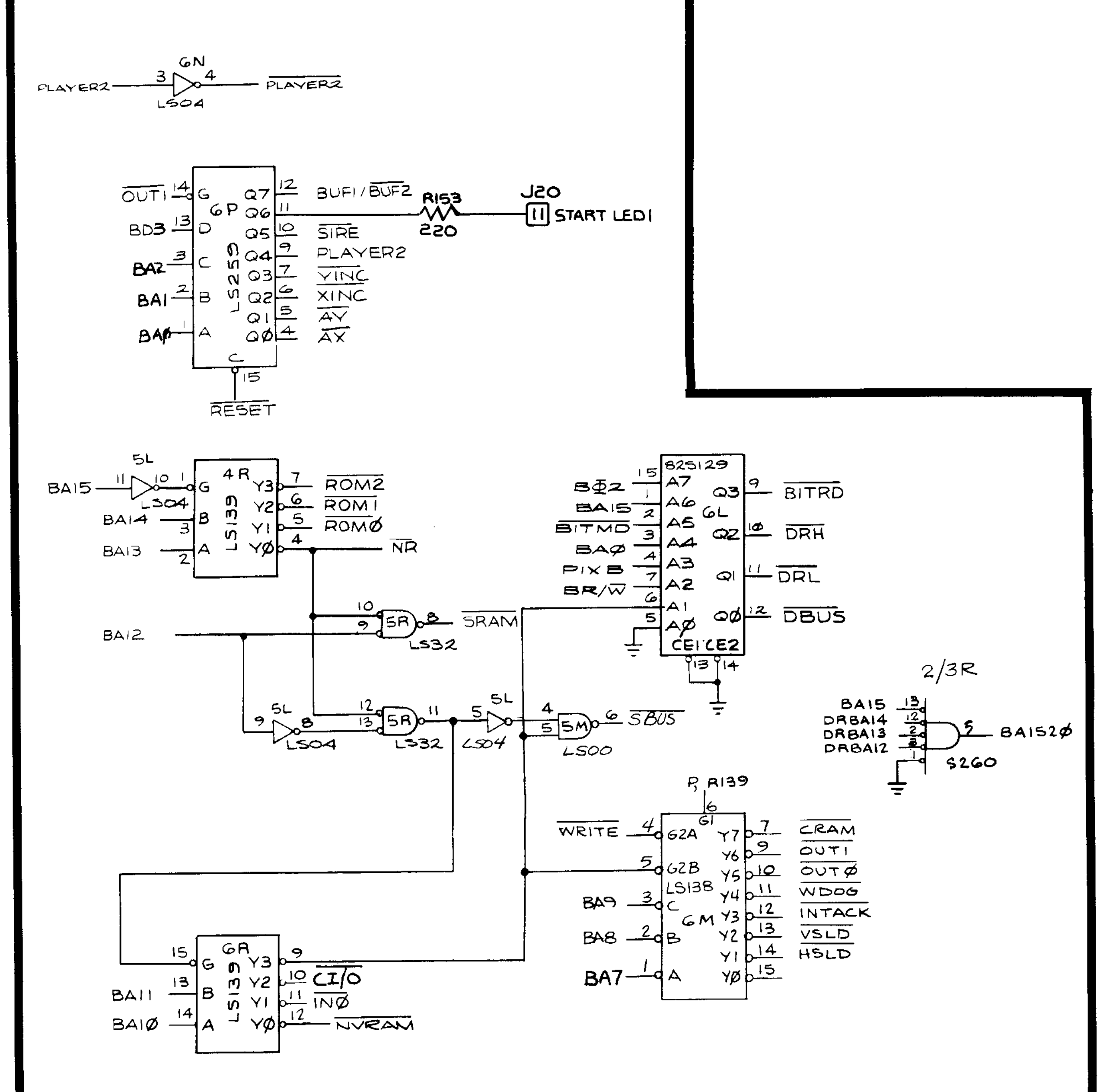
Crystal Castles PCB Schematic Diagram

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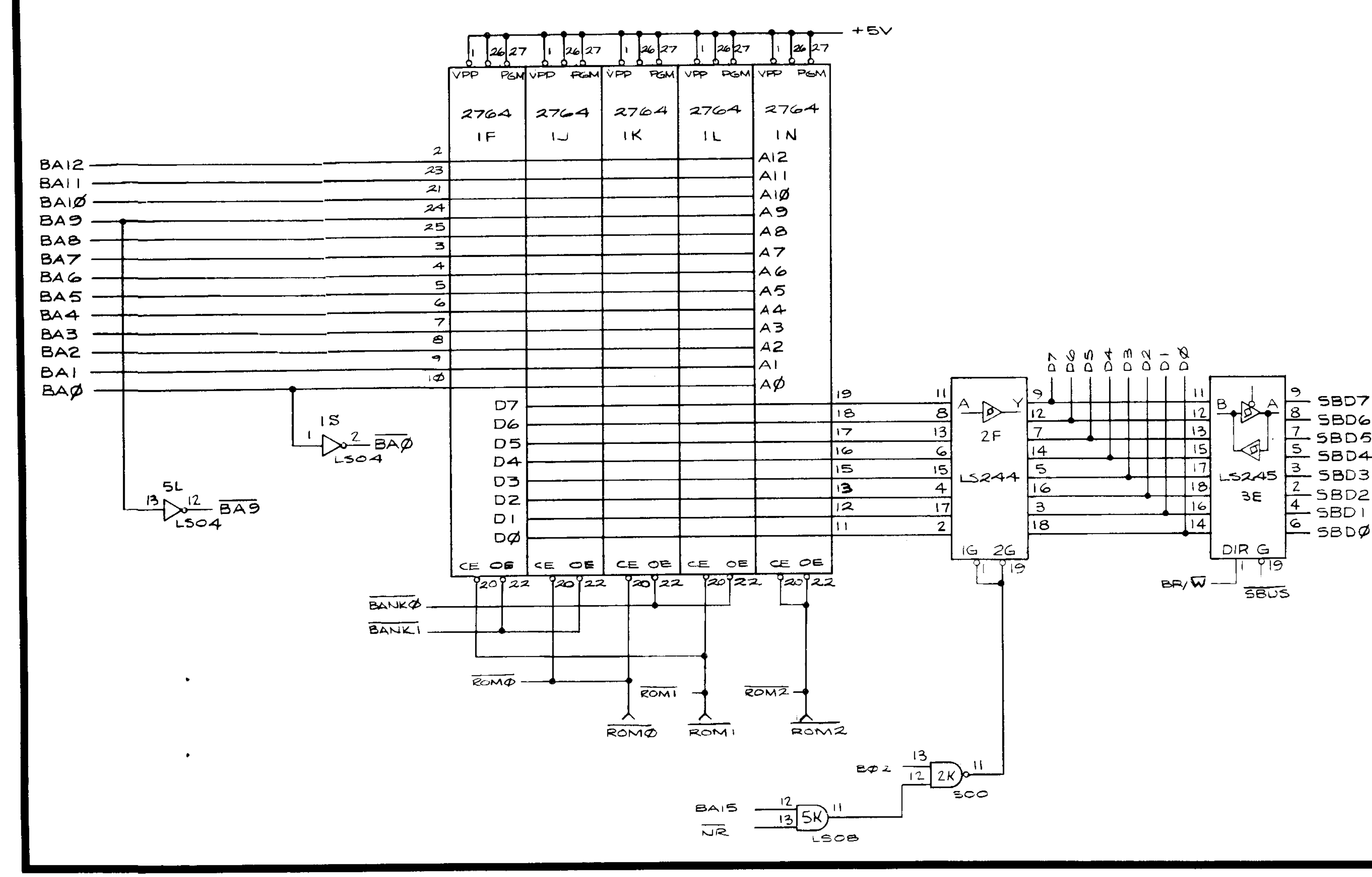
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Address Decoders



Program Memory



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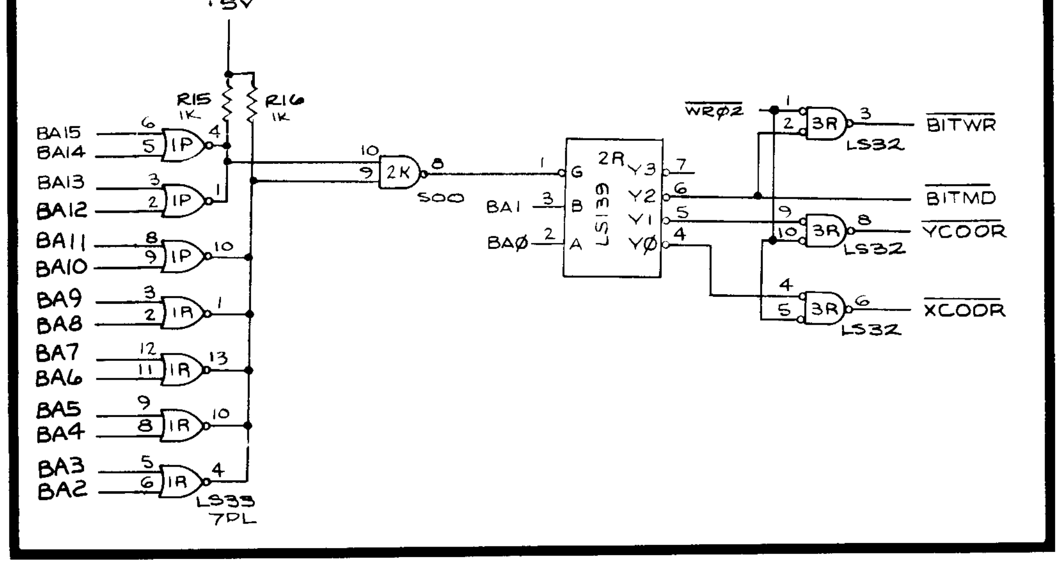
Crystal Castles PCB Schematic Diagram

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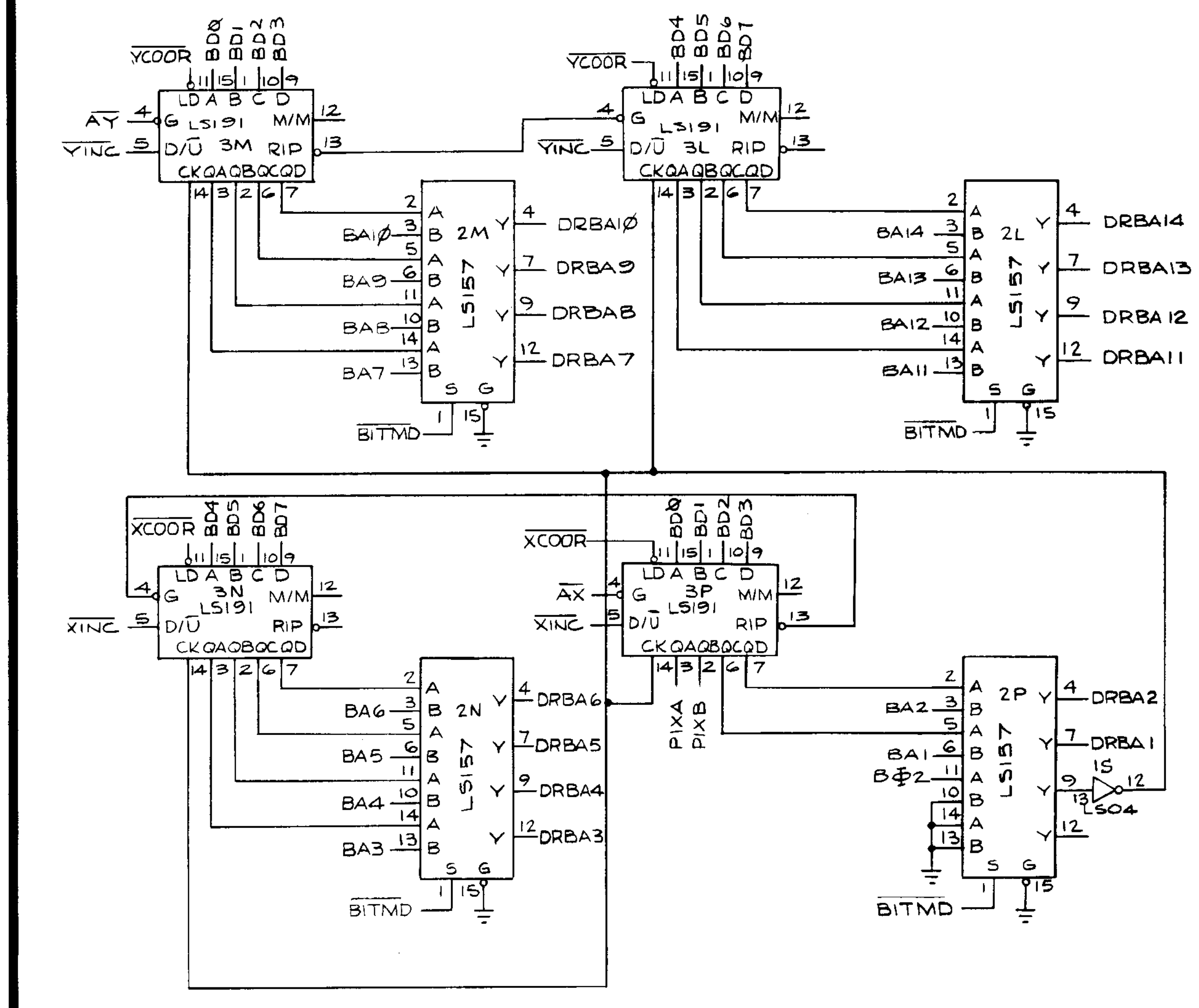
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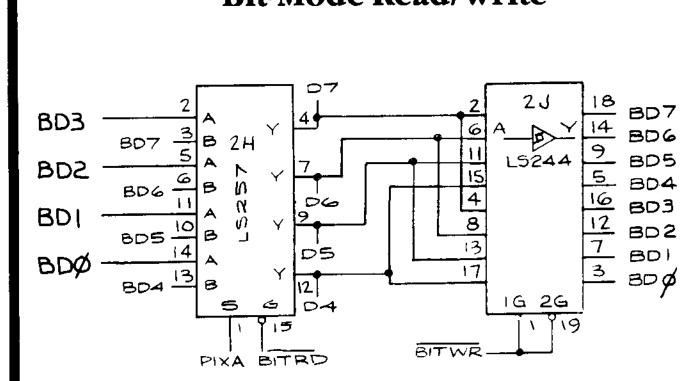
Bit-Mode Decoder



Auto Increment



Bit-Mode Read/Write



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Crystal Castles PCB Schematic Diagram

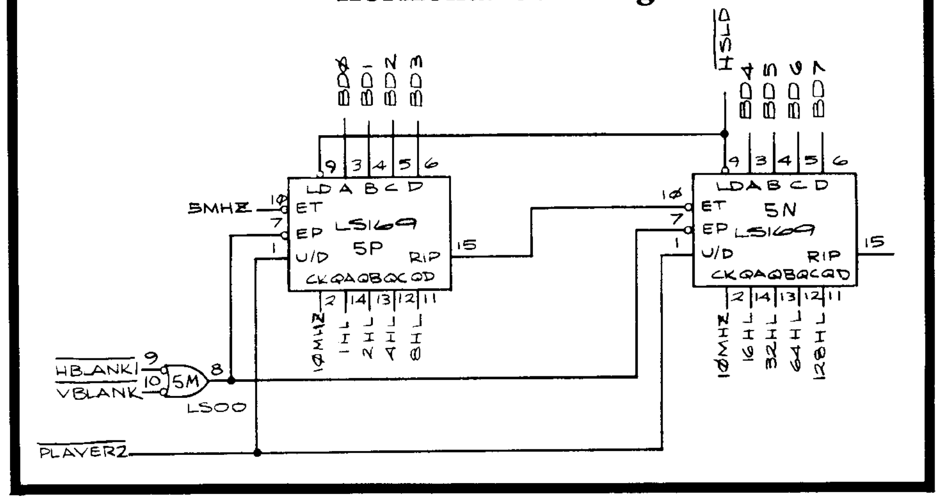
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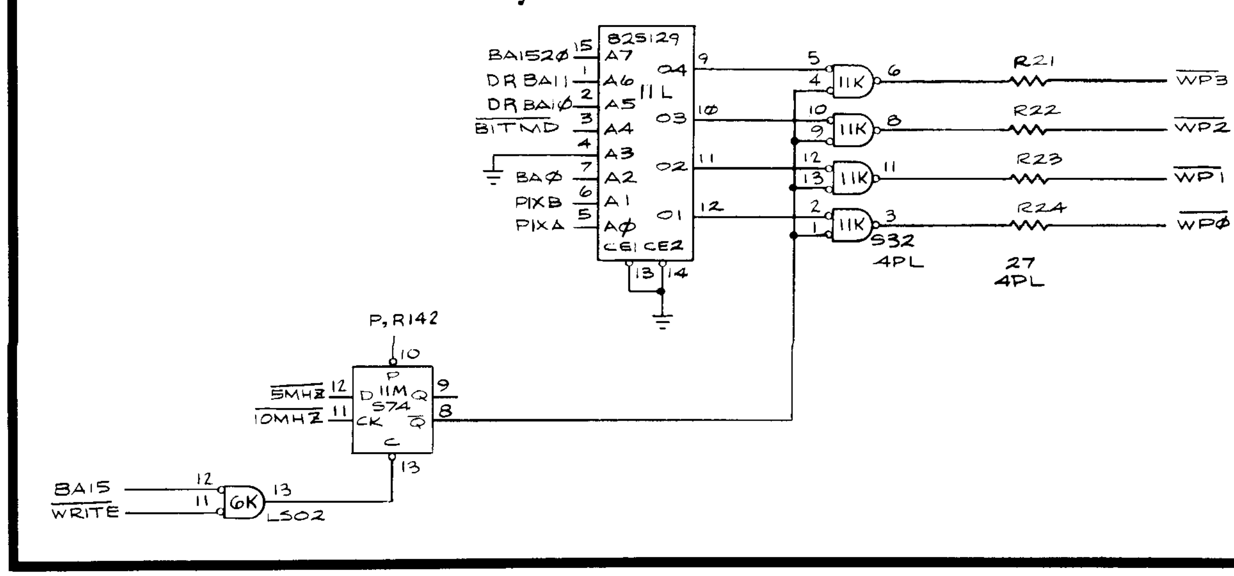
SP-241 Sheet 5A

2nd printing

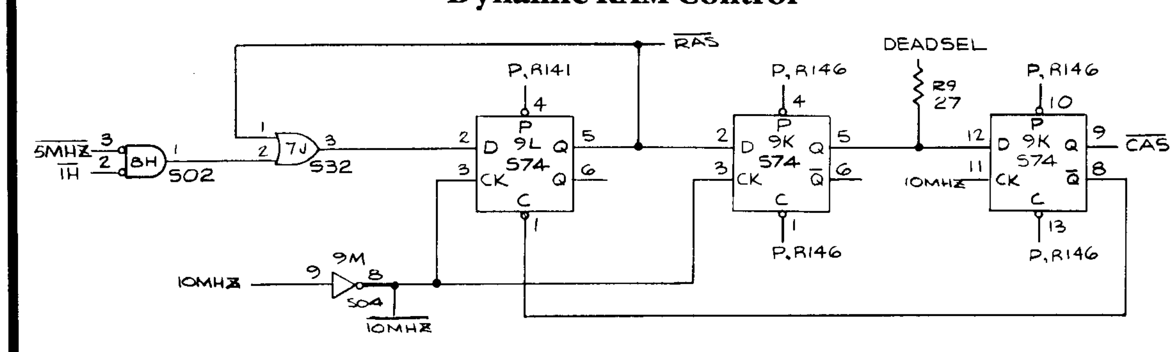
Horizontal Scrolling



Dynamic RAM Write Protection



Dynamic RAM Control

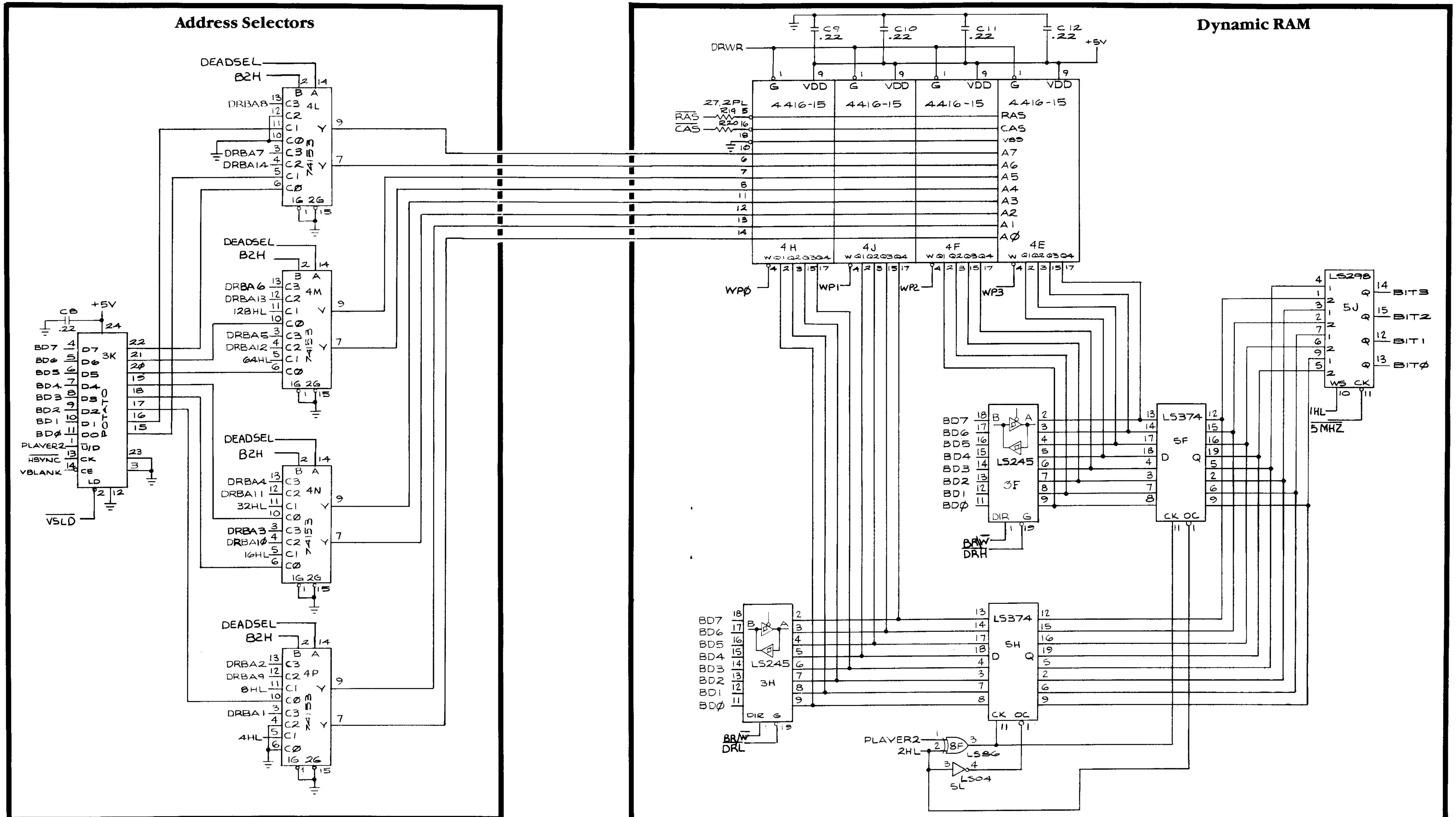


Crystal Castles PCB Schematic Diagram

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Crystal Castles PCB Schematic Diagram

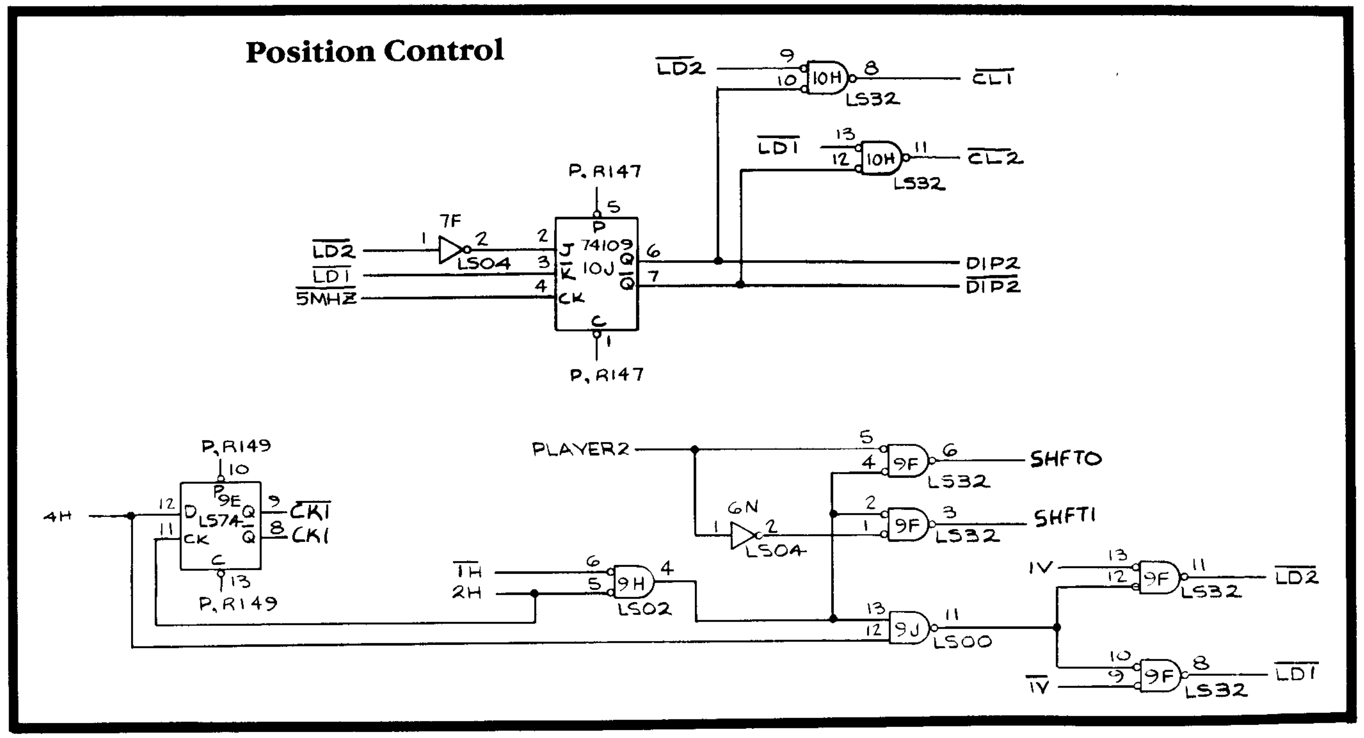
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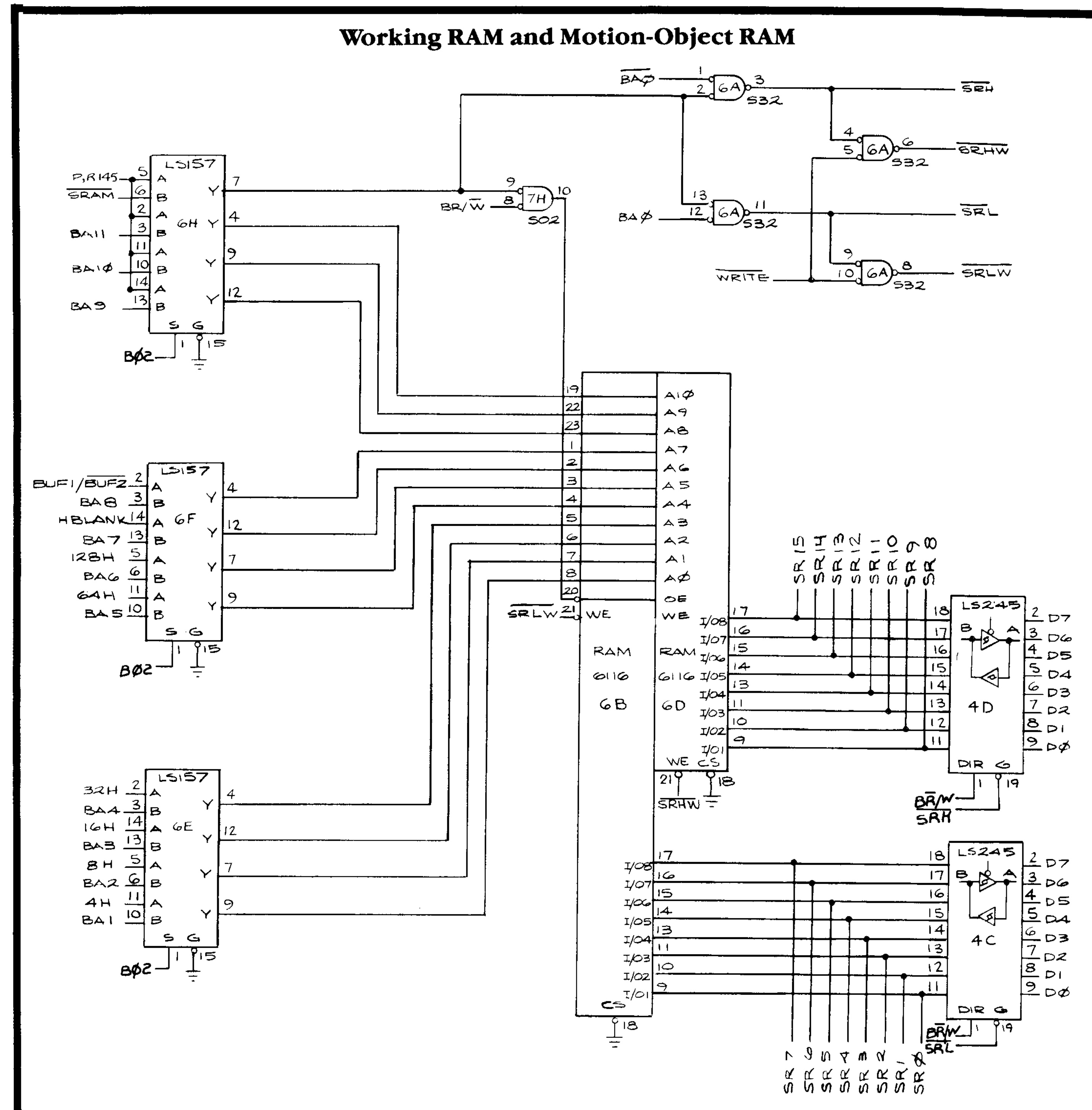
SP-241 Sheet 6A

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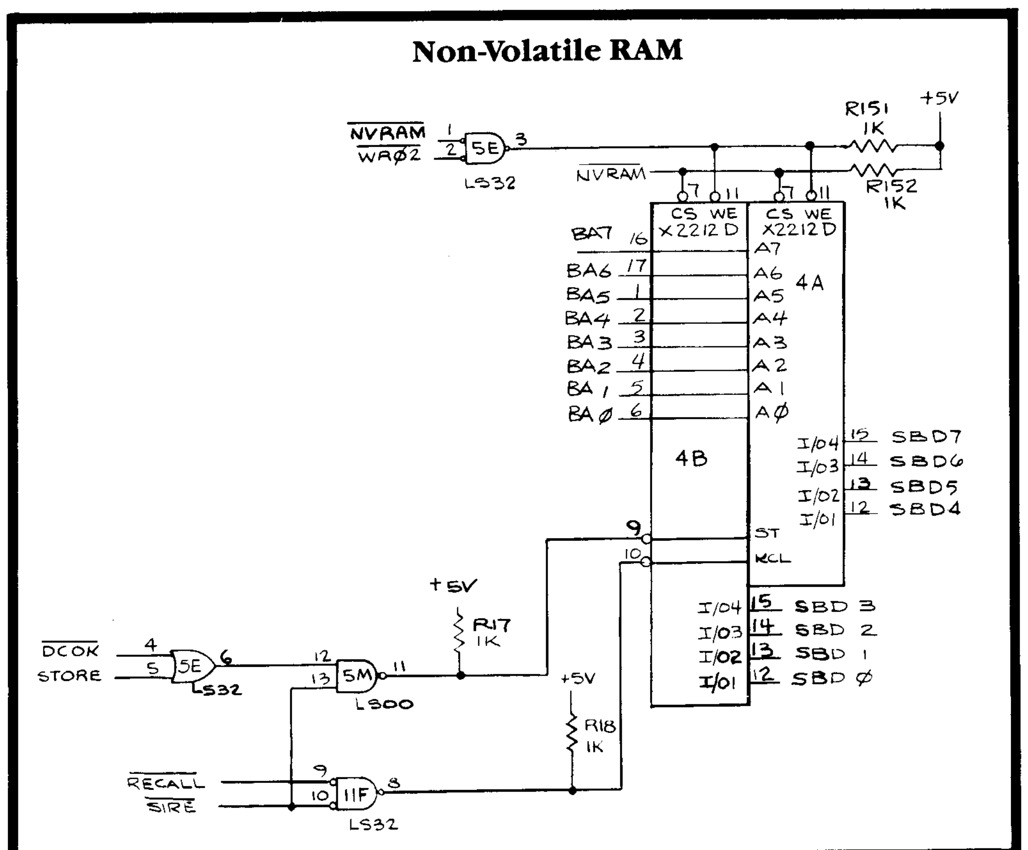
Position Control



Working RAM and Motion-Object RAM



Non-Volatile RAM

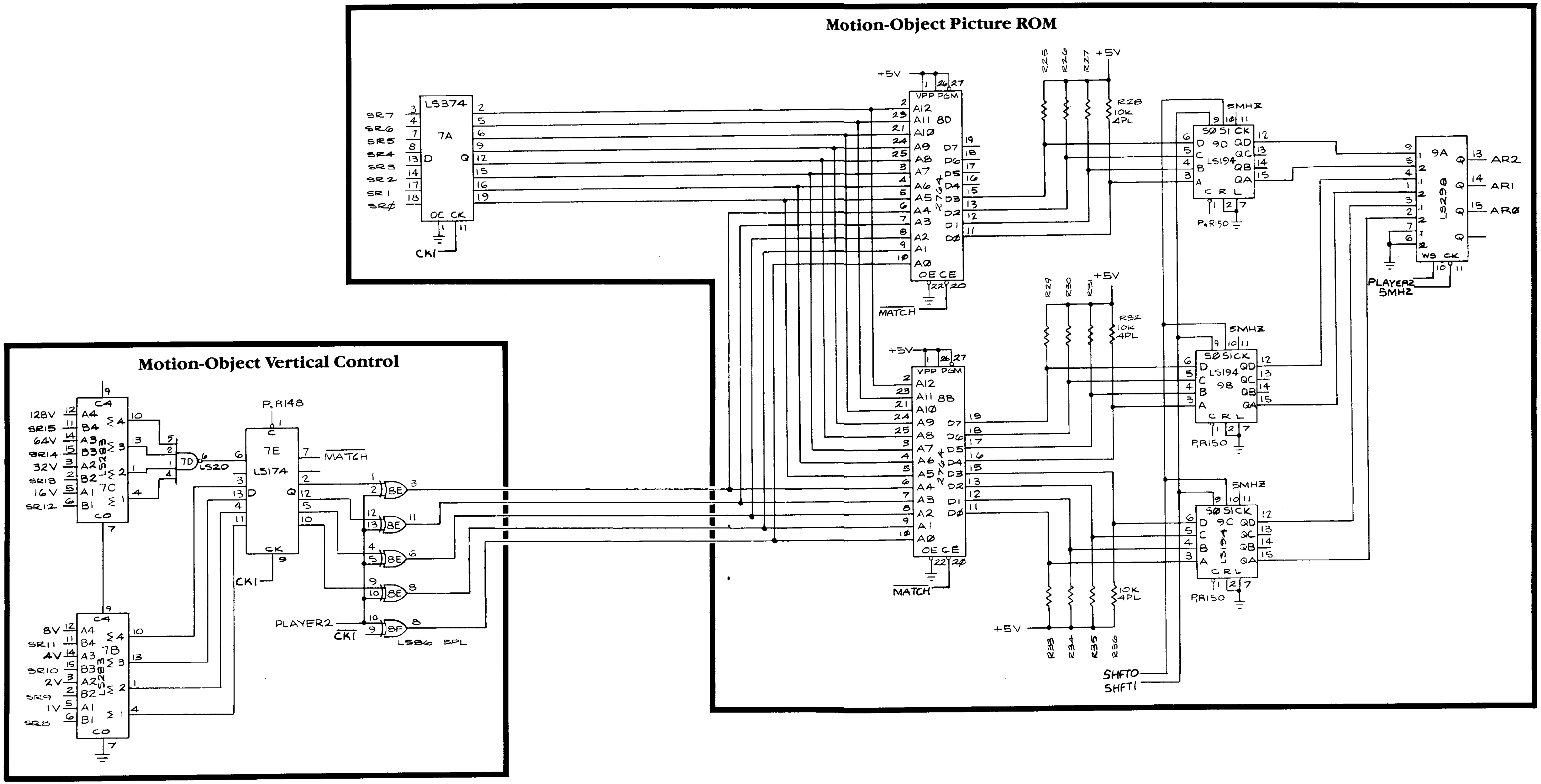


Crystal Castles PCB Schematic Diagram

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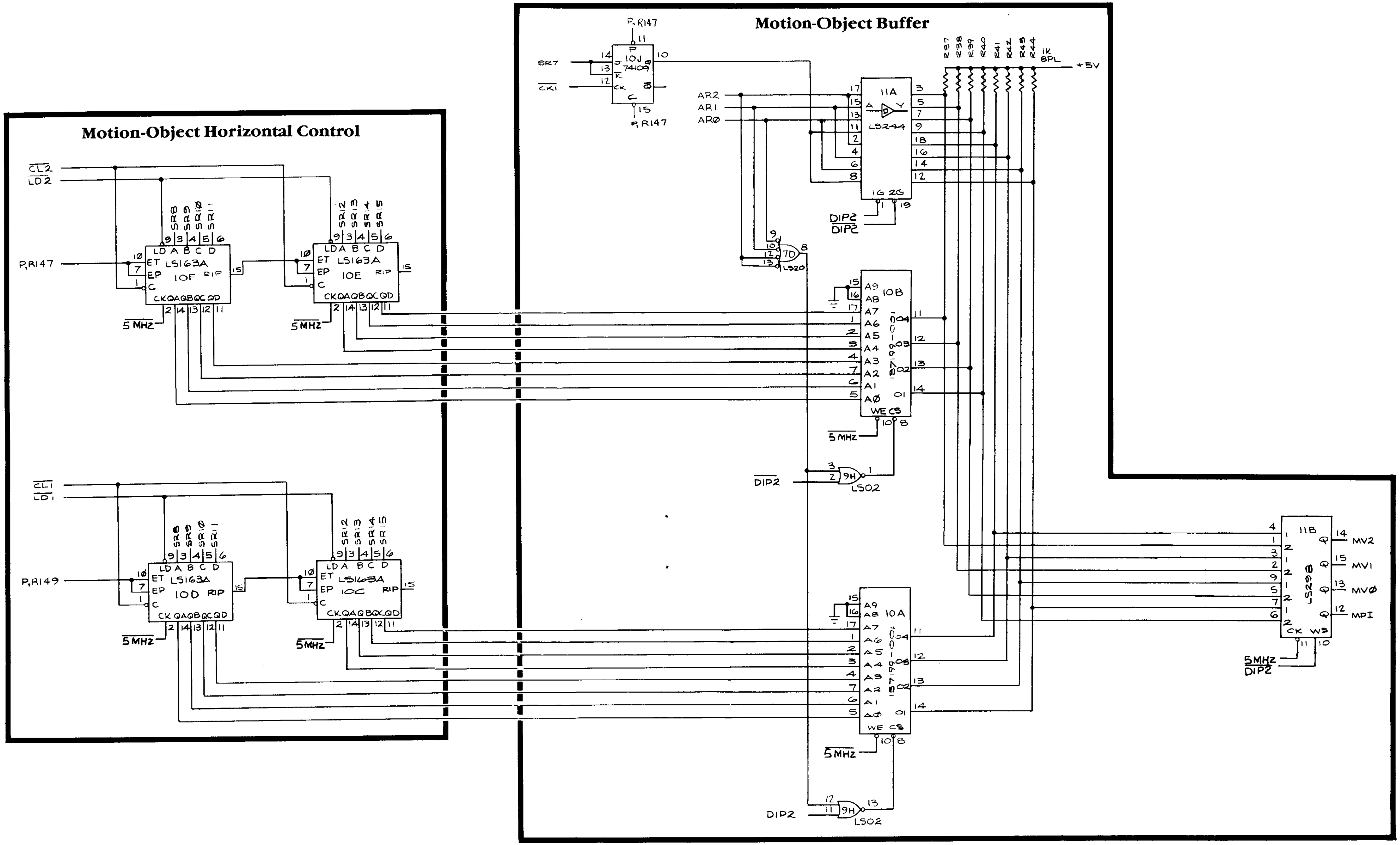


Crystal Castles PCB Schematic Diagram

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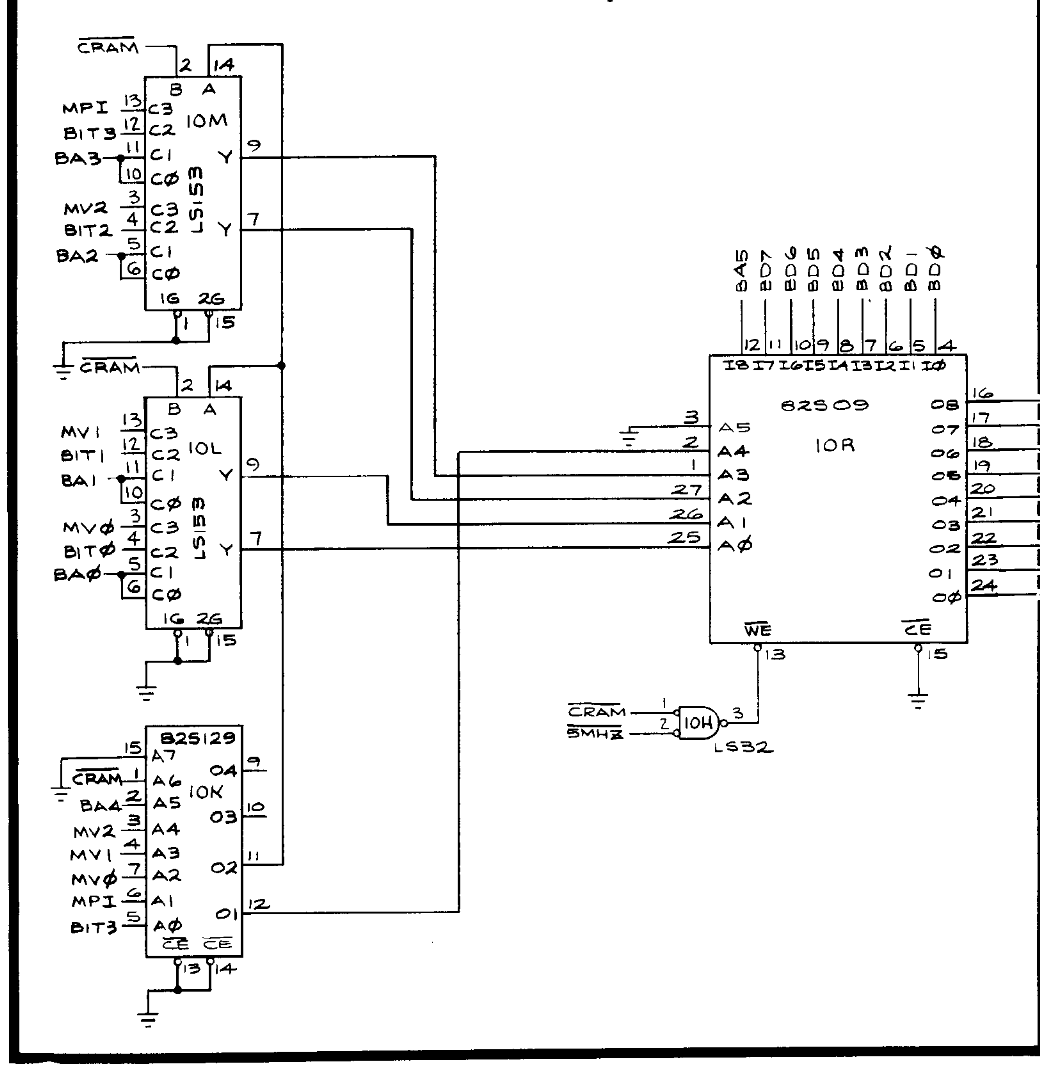
Crystal Castles PCB Schematic Diagram

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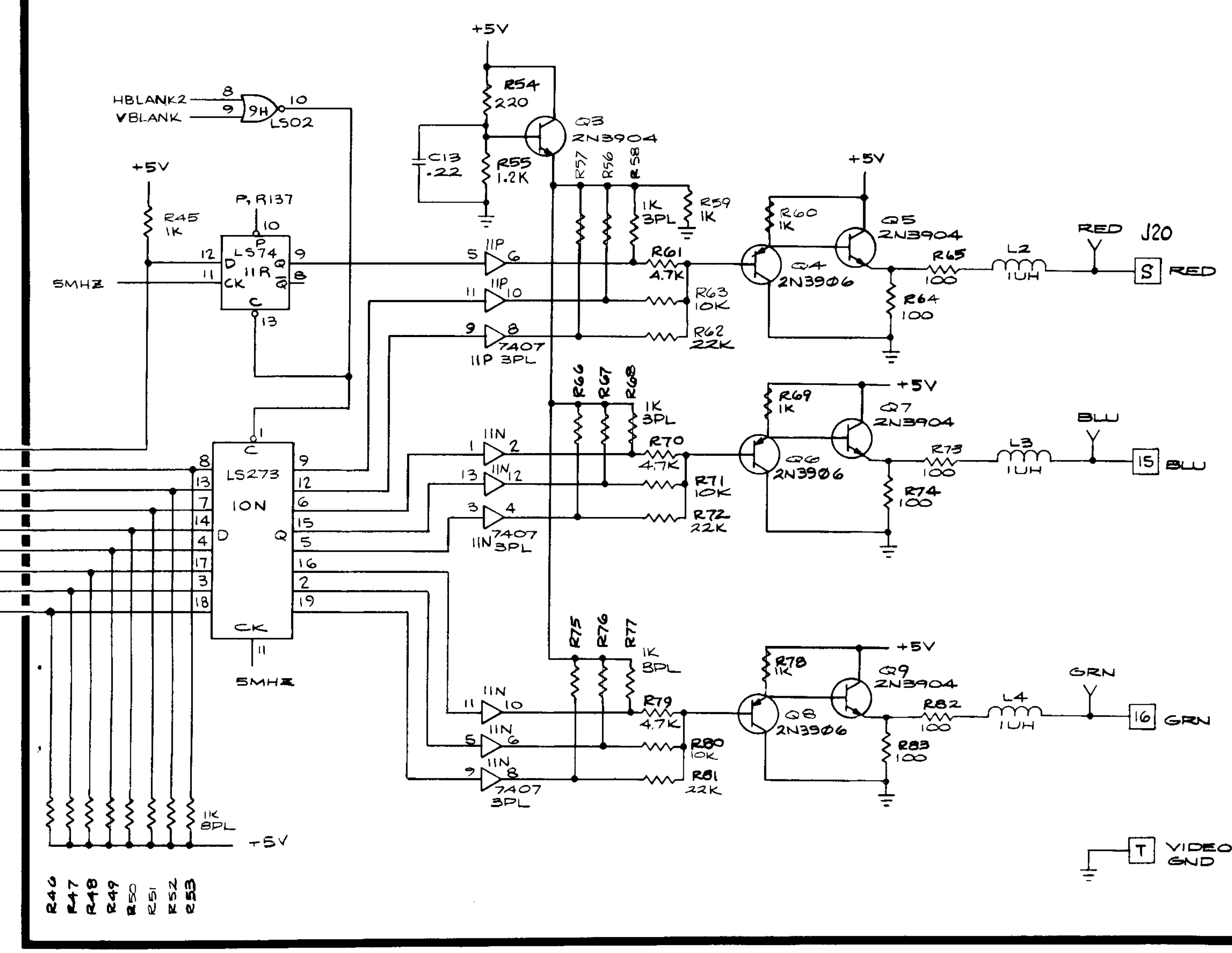
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Color Memory



Color Output



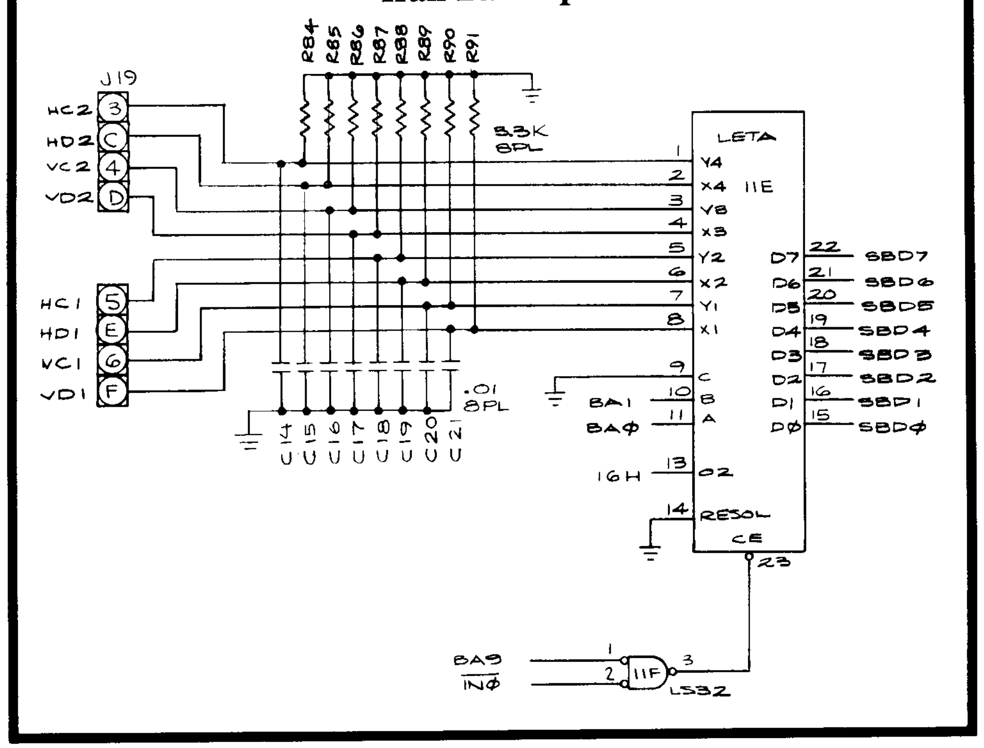
Crystal Castles PCB Schematic Diagram

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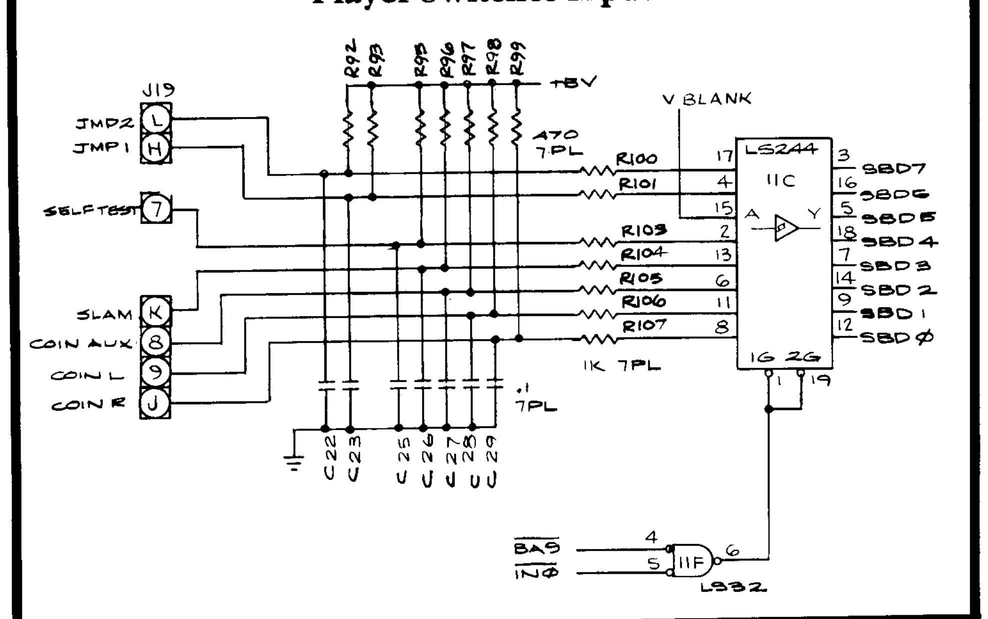
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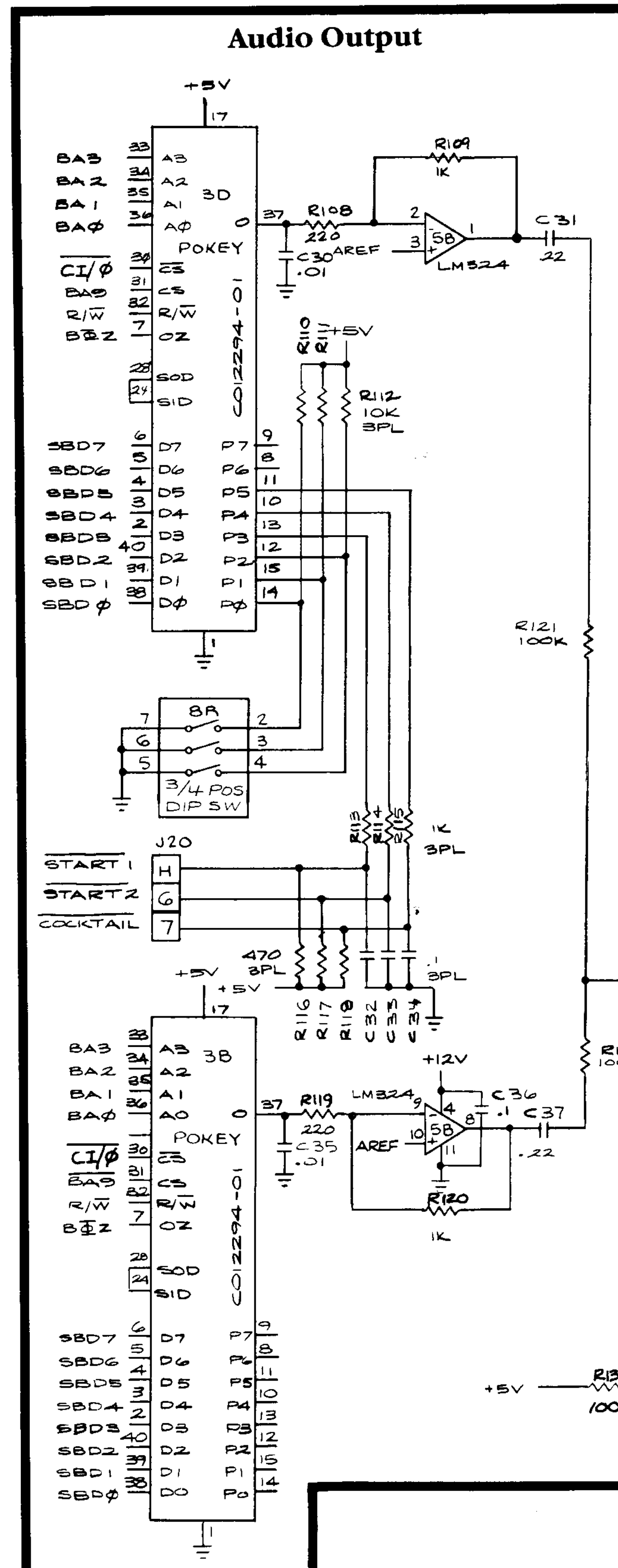
Trak-Ball Input

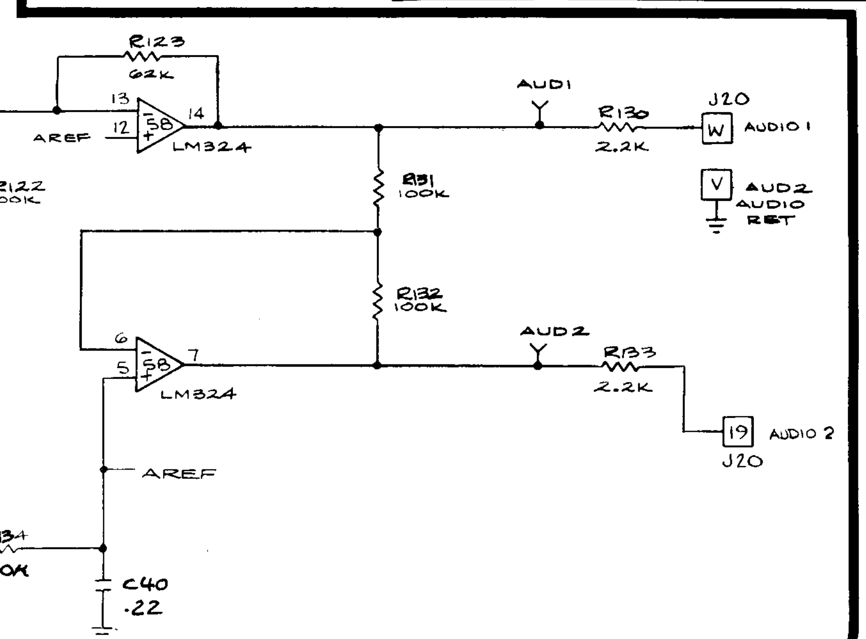


Player Switches Input

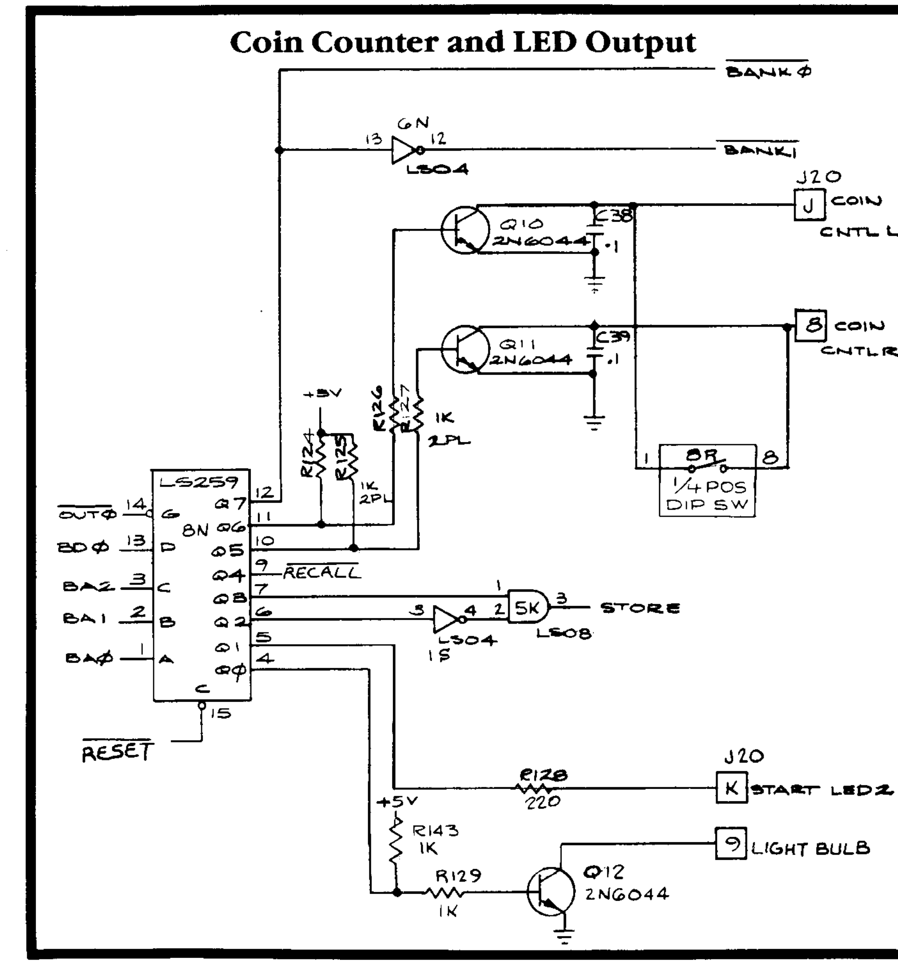


Audio Output





Coin Counter and LED Output

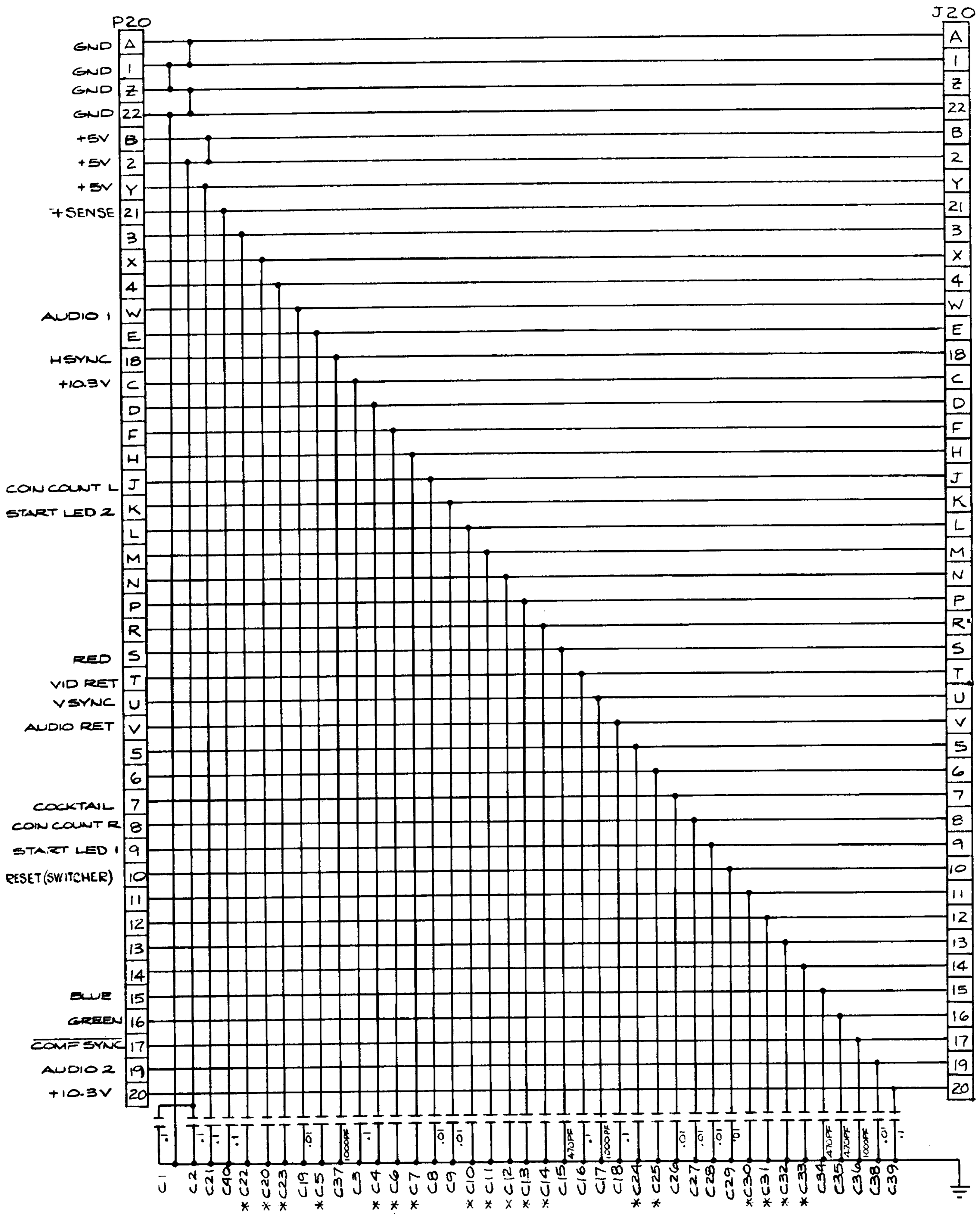


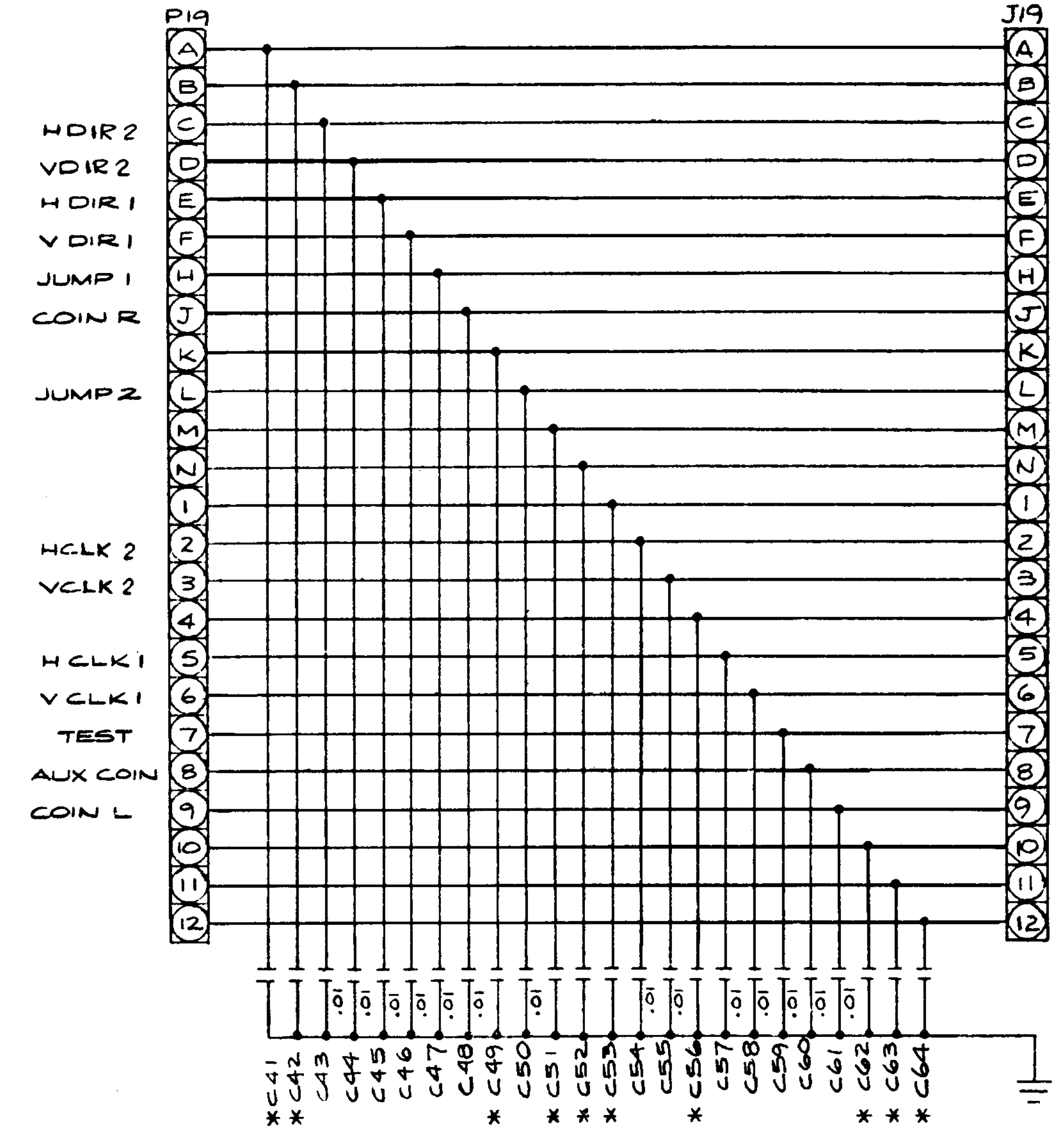
Crystal Castles PCB Schematic Diagram

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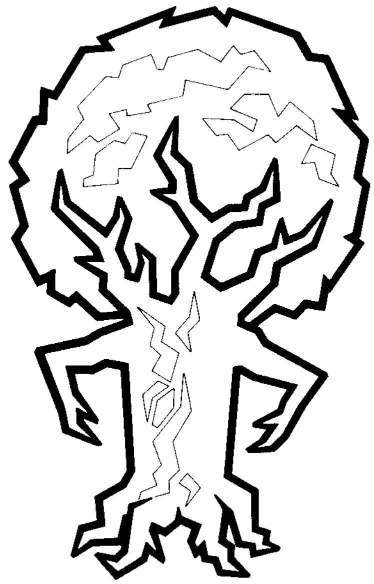
NOTES:
1. * DENOTES NOT LOADED CAPACITOR.

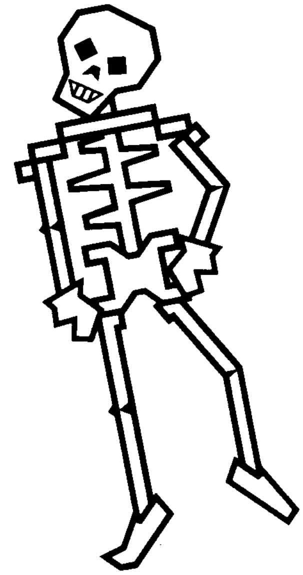
Crystal Castles EMI Shield PCB

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Crystal Castles™ Troubleshooting Guide

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Crystal Castles™
Troubleshooting with the CAT Box

Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor 2C from the game PCB.
5. Connect the harness from the game to the game PCB.
6. Connect together the $\Phi 0$ and $\Phi 2$ test points on the game PCB with the shortest possible jumper.
7. Connect the $\overline{WDDIS}$ test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/$\overline{W}$
11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

B. Checking the Address Lines

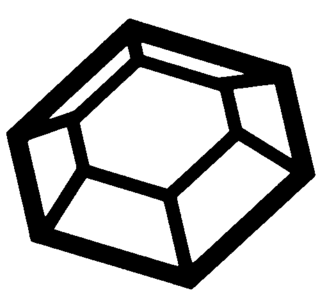
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES: 1
    b. PULSE MODE: UNLATCHED
    c. R/$\overline{W}$ MODE: (OFF)
    d. R/$\overline{W}$: READ
3. Key in the address pattern given in Table 1 (use AAAA to start) with the CAT Box keyboard.
4. Set R/$\overline{W}$ MODE to STATIC.
5. Probe each IC-pin listed in Table 1 with the DATA PROBE and check that the CAT Box 1 or 0 LED for the corresponding address line lights up.
6. Repeat parts 2-c through 5 using address 5555 in part 3.

Table 1 Address Lines

Logic State for Address AAAA	IC-Pin	Logic State for Address 5555
BA15 1	1B3	0
BA14 0	1B5	1
BA13 1	1B7	0
BA12 0	1B9	1
BA11 1	1B12	0
BA10 0	1B14	1
BA9 1	1B16	0
BA8 0	1B18	1
BA7 1	1C9	0
BA6 0	1C7	1
BA5 1	1C5	0
BA4 0	1C3	1
BA3 1	1C12	0
BA2 0	1C14	1
BA1 1	1C16	0
BA0 0	1C18	1

C. Checking the Data Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES:1
    b. R/$\overline{W}$ MODE: (OFF)
    c. R/$\overline{W}$: WRITE
3. Key in address 0000 with the keyboard.
4. Press DATA SET. Key in data AA with the keyboard.
5. Set R/$\overline{W}$ MODE to STATIC.
6. Probe each IC-pin listed in Table 2 with the DATA PROBE and check that the CAT Box 1 or 0 LED for the corresponding address line lights up.
7. Set R/$\overline{W}$ MODE to (OFF).
8. Repeat parts 4 through 6 using data 55 in part 4.



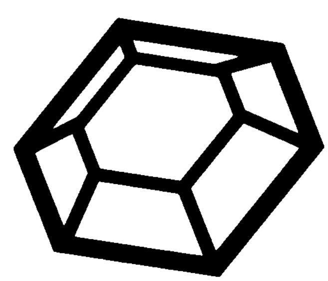


Table 2 Data Lines

Logic State for Data AA	IC-Pin	Logic State for Data 55
D7 1	2E-11	0
D6 0	2E-12	1
D5 1	2E-13	0
D4 0	2E-14	1
D3 1	2E-15	0
D2 0	2E-16	1
D1 1	2E-17	0
D0 0	2E-18	1
BD7 1	2E-9	0
BD6 0	2E-8	1
BD5 1	2E-7	0
BD4 0	2E-6	1
BD3 1	2E-5	0
BD2 0	2E-4	1
BD1 1	2E-3	0
BD0 0	2E-2	1

D. Checking the RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES:1024
   c. R/$\overline{W}$ MODE: (OFF)
   d. R/$\overline{W}$: WRITE
3. Enter address 0003 with the keyboard.
4. Set the CAT Box switches as indicated:
   a. R/$\overline{W}$ MODE to PULSE and back to (OFF)
   b. R/$\overline{W}$ to READ
   c. R/$\overline{W}$ MODE to PULSE and back to (OFF)
5. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.
6. Repeat this test with DBUS SOURCE set to ADDR.
7. Set the CAT Box switches as indicated:
   a. BYTES: 256
   b. DBUS SOURCE: ADDR
   c. R/$\overline{W}$: (OFF)
   d. R/$\overline{W}$: WRITE
8. Repeat parts 5 through 6 to check addresses from 1000 through 8FFF.

NOTE

The two custom audio I/O chips must be tested separately by performing the self-test, substituting a known good part, or performing the following procedure.

E. Checking the Custom Audio I/O Chips

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/$\overline{W}$ to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

Address	Data	Test Results
98 98 98 98	00 03 55 AF	Custom Audio I/O Chip 4D channel 1 produces pure tone.
98	00	Custom Audio I/O Chip 4D channel 1 turns off.
98 98	55 AF	Custom Audio I/O Chip 4D channel 2 produces pure tone.
98	00	Custom Audio I/O Chip 4D channel 2 turns off.
9A 9A 9A 9A	00 03 55 AF	Custom Audio I/O Chip 4B channel 1 produces pure tone.
9A	00	Custom Audio I/O Chip 4B channel 1 turns off.
9A 9A	55 AF	Custom Audio I/O Chip 4B channel 2 produces pure tone.
9A	00	Custom Audio I/O Chip 4B channel 2 turns off.

F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{\text{W}}$: WRITE
   c. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter address 9600 with the keyboard.
4. Press DATA SET and enter data FF with the keyboard.
5. Set R/$\overline{\text{WE}}$ to PULSE and back to (OFF).
6. For each entry listed in Table 4, do the following:
   a. Set R/$\overline{\text{W}}$ MODE to (OFF).
   b. Set R/$\overline{\text{W}}$WRITE.
   c. Enter the first address with the keyboard.
   d. Press DATA SET and enter the data for that address with the keyboard.
   e. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
   f. Set R/$\overline{\text{W}}$ to READ.
   g. Enter the next address.
   h. Set R/$\overline{\text{W}}$ MODE to STATIC.
   i. Activate the input switch or signal indicated in Table 4 and check the test result.
   j. Set R/$\overline{\text{W}}$ MODE to (OFF).
   k. Repeat parts g through j for each subsequent address given for the entry.

Table 4 Player Switches, Option Switches, and Trak-Ball™ Inputs

Address	Input Switches/Signals	Test Results
9400	Trak-Ball™ VERT	
9401	Trak-Ball™ HORIZ	
9402	Trak-Ball™ VERT (Player 2)	
9403	Trak-Ball™ HORIZ (Player 2)	
9600	D0 COIN R	
	D1 COIN L	
	D2 COIN AUX	
	D3 SLAM	
	D4 SELF TEST	
	D5 SPARE	
	D6 JMP1	
	D7 JMP2	
00–9A0B	SW2 D0	Read switches at address 9A08. DATA display changes when any of these switches or signals are activated.
	SW3 D1	
	SW4 D2	

G. Checking the Coin Counter and Trak-Ball Light

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{\text{W}}$: WRITE
   d. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter the address in Table 5 with the keyboard.

CAUTION

If you write ON data to activate a solenoid, *deactivate the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each address listed in Table 5, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter the ON data with the keyboard.
      - Set R/$\overline{\text{W}}$ MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter the OFF data with the keyboard.
      - Set R/$\overline{\text{W}}$ MODE to STATIC and back to (OFF).

Table 5 LED and Coin Counter Outputs

Address	On Data	Off Data	Output Device
9E86	FF	00	Left Coin Counter
9E85	FF	00	Right Coin Counter
9E80	FF	00	Trak-Ball™ Light



Troubleshooting the Watchdog Circuit

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the RESET line.

$\overline{\text{RESET}}$ is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the $\overline{\text{RESET}}$ test point is grounded. A pulsing $\overline{\text{RESET}}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{\text{RESET}}$ signal indicates a problem exists somewhere within the microprocessor circuitry. To aid in troubleshooting, the $\overline{\text{WDDIS}}$ test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition.

